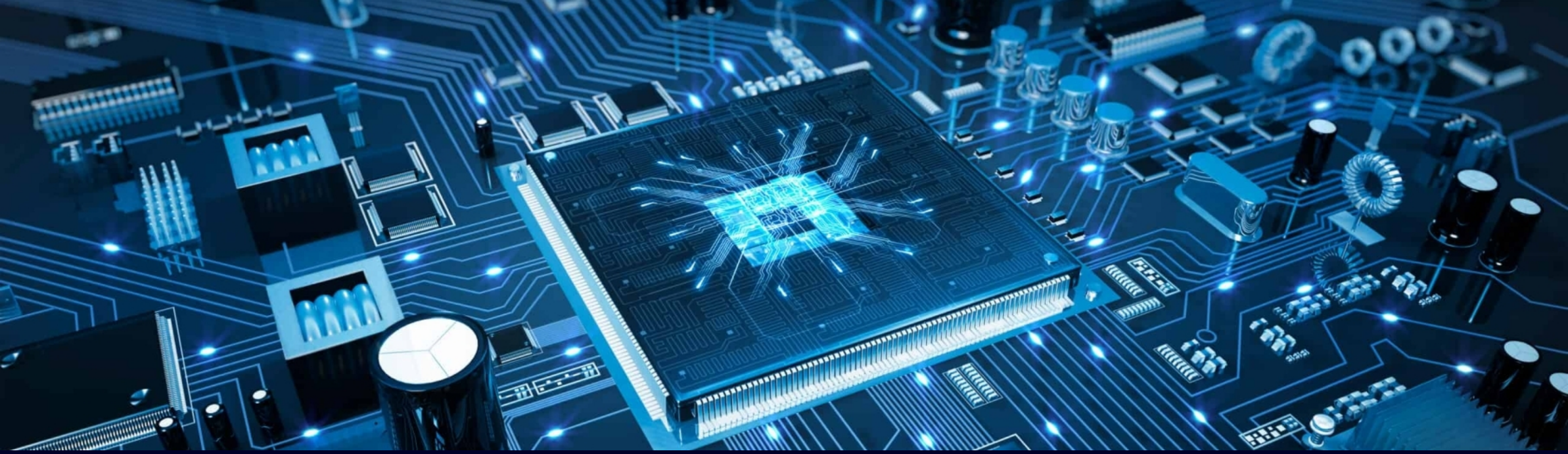

Tessent™ UltraSight-V

An On-chip Debug and Trace Solution for RISC-V Systems

Yifan Li, Account Technology Manager

Tessent Products

Siemens EDA

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Traditional SoC Debug Needs Help

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The time and costs taken to debug and optimize software executing on complex RISC-V based SoCs are escalating

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Low debug productivity

Identifying hardware and real-time software issues require more efficient methods to observe, to debug, to iterate, and to scale

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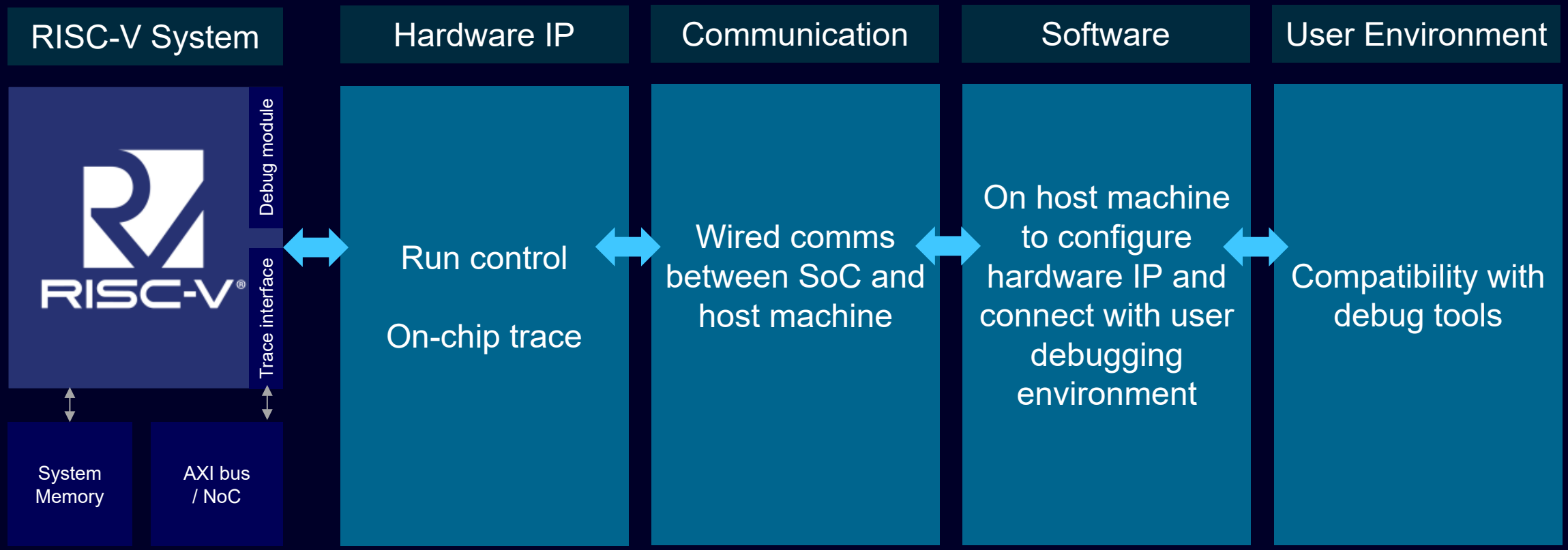
Growing Markets Demand Scalable Debug Solution



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Growing Markets Demand Pre-verified IP Solution

~50%

Mean ASIC project time spent in verification

"Projects spending minimal time typically reuse pre-verified IP modules, reducing verification overhead."

"Conversely, projects with significant verification time often involve high proportions of newly developed IP"

By 2024 Wilson Research Group IC/ASIC functional verification trend report

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End-to-end RISC-V Debug & Trace Solution

Scalable to

System-wide Debug

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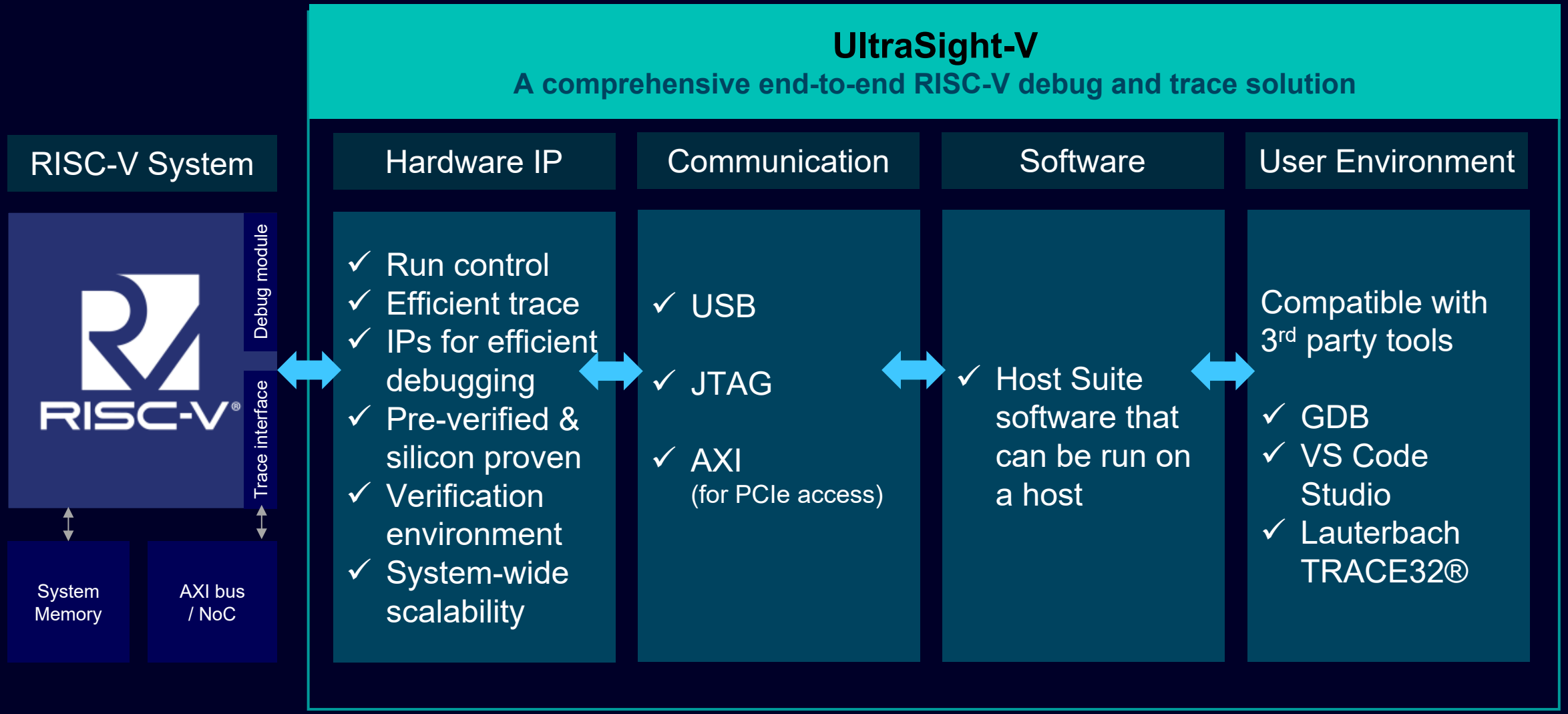
Tessent UltraSight-V



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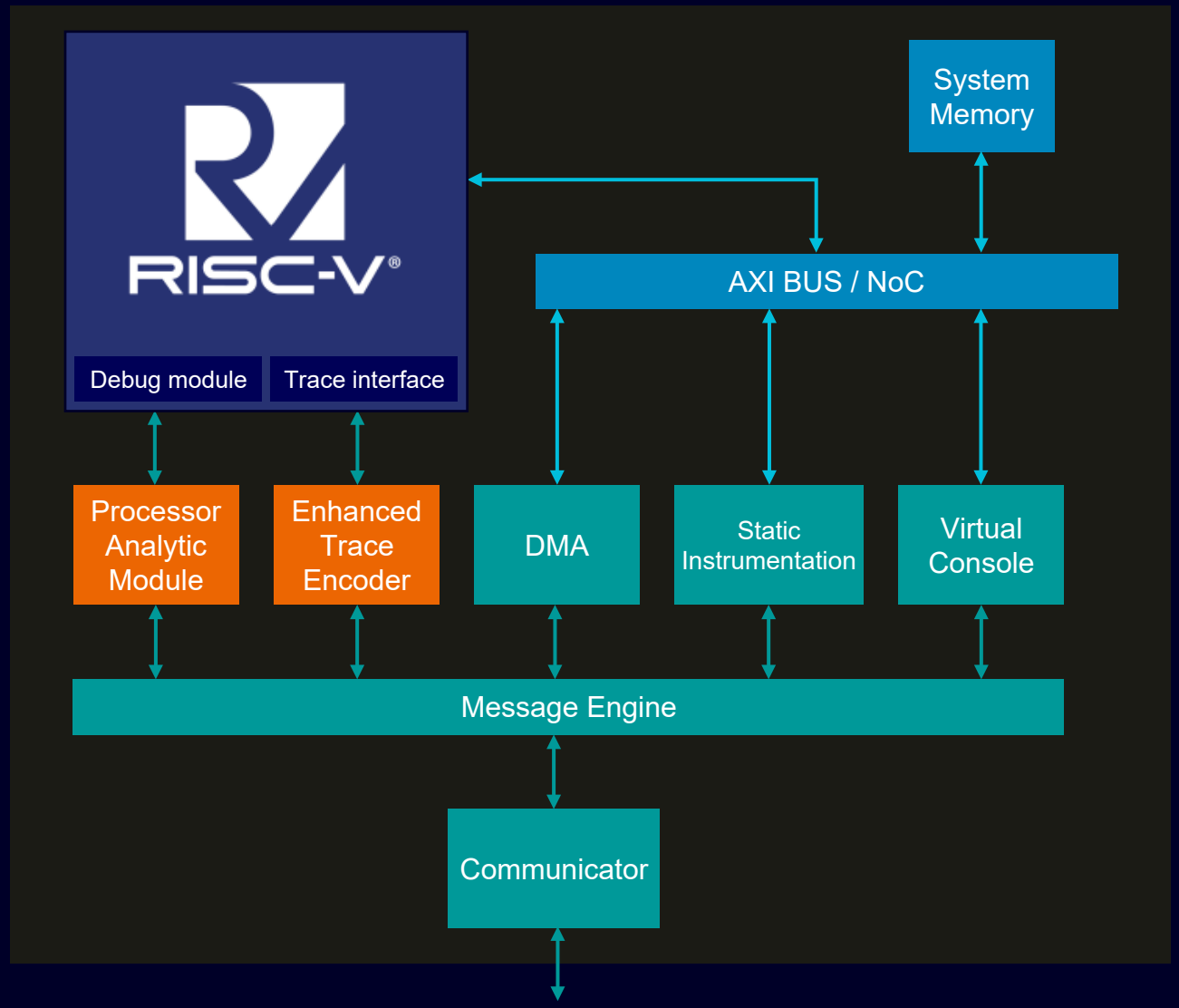
Hardware IPs to Debug RISC-V Cores

- Processor Analytic Module
  - Provides run control capabilities
- Enhanced Trace Encoder
  - Outputs processor trace (E-Trace)



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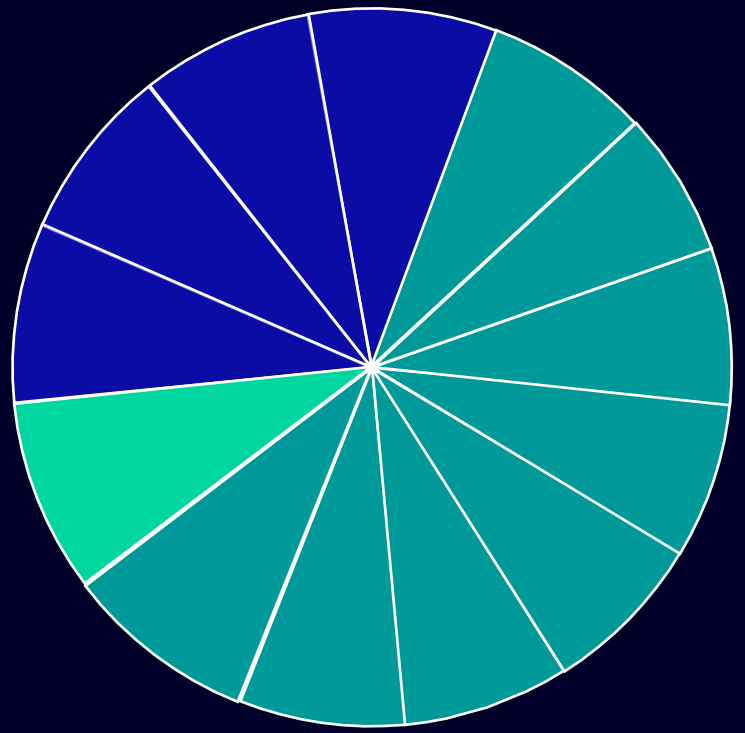
Enhanced Trace Encoder IP

RISC-V Trace mandatory features

- Instruction trace
- Hart to encoder interface
- ‘Delta Address’ trace mode
- Efficient packet format



RISC-V Trace optional extensions

- Multiple instruction retirement
- Sequentially inferable jump mode
- Implicit return mode
- Branch Prediction mode
- Jump Target Cache mode
- Full Address mode
- Sign-based compression
- Filtering

Tessent Embedded Analytics

- Cycle accurate trace

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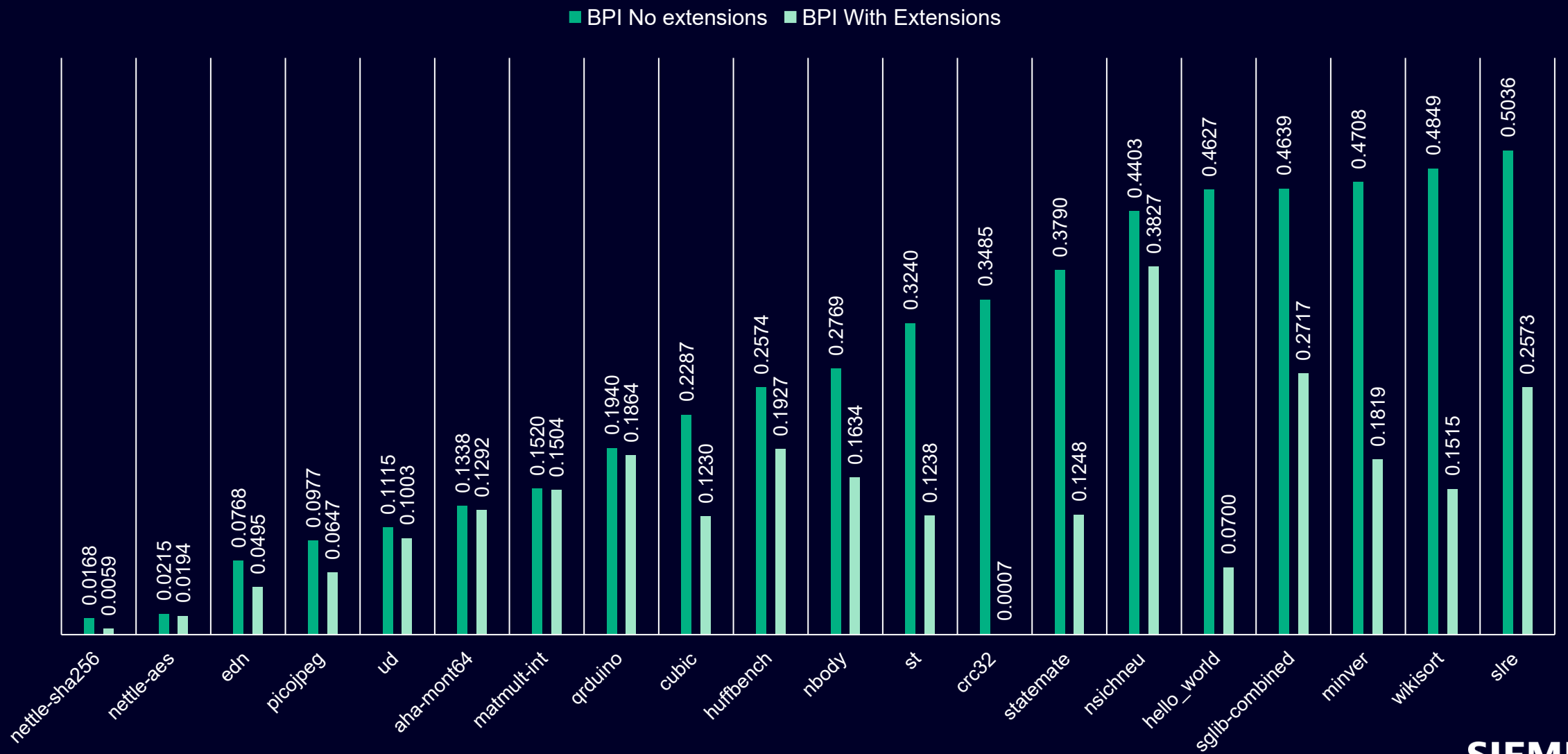
Trace Compression - Embench™ Benchmark Results

~40% BPI improvement with optional extensions



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Hardware IPs for Efficient Debugging

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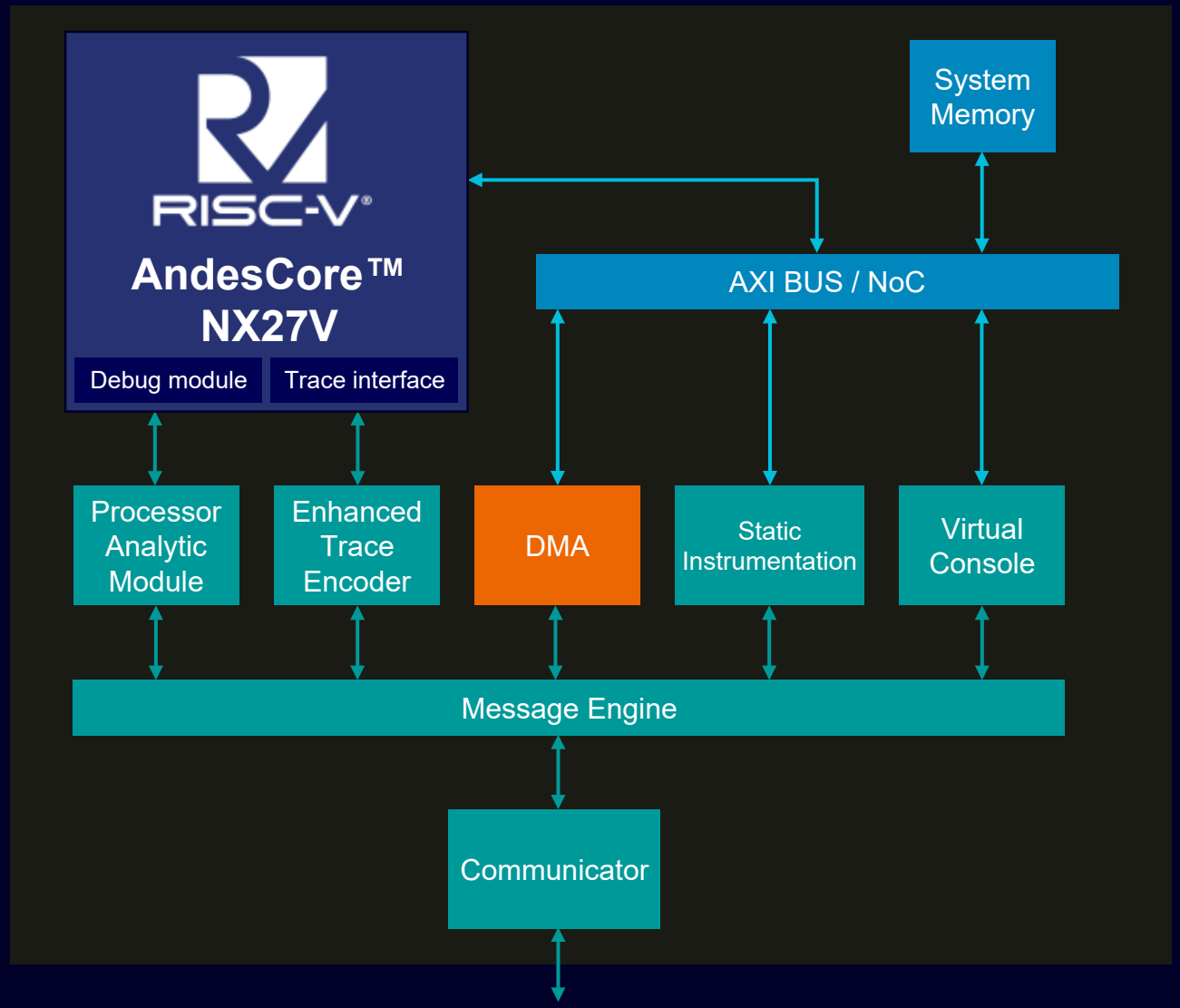
Hardware IPs for Efficient Debugging

Hardware IPs (Parametrized RTL)

- DMA
  - Fast memory access



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Hardware IPs for Efficient Debugging

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- DMA
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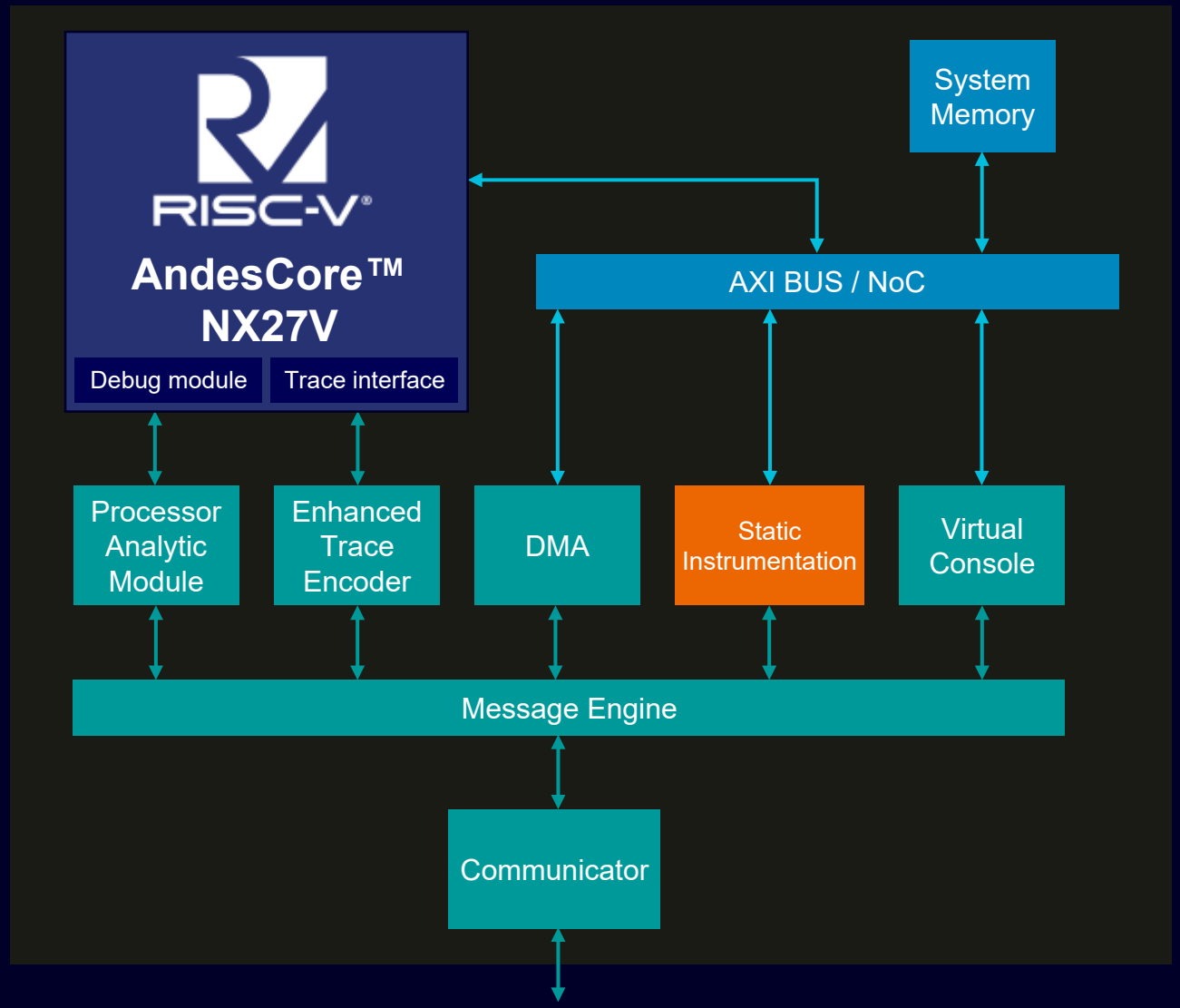

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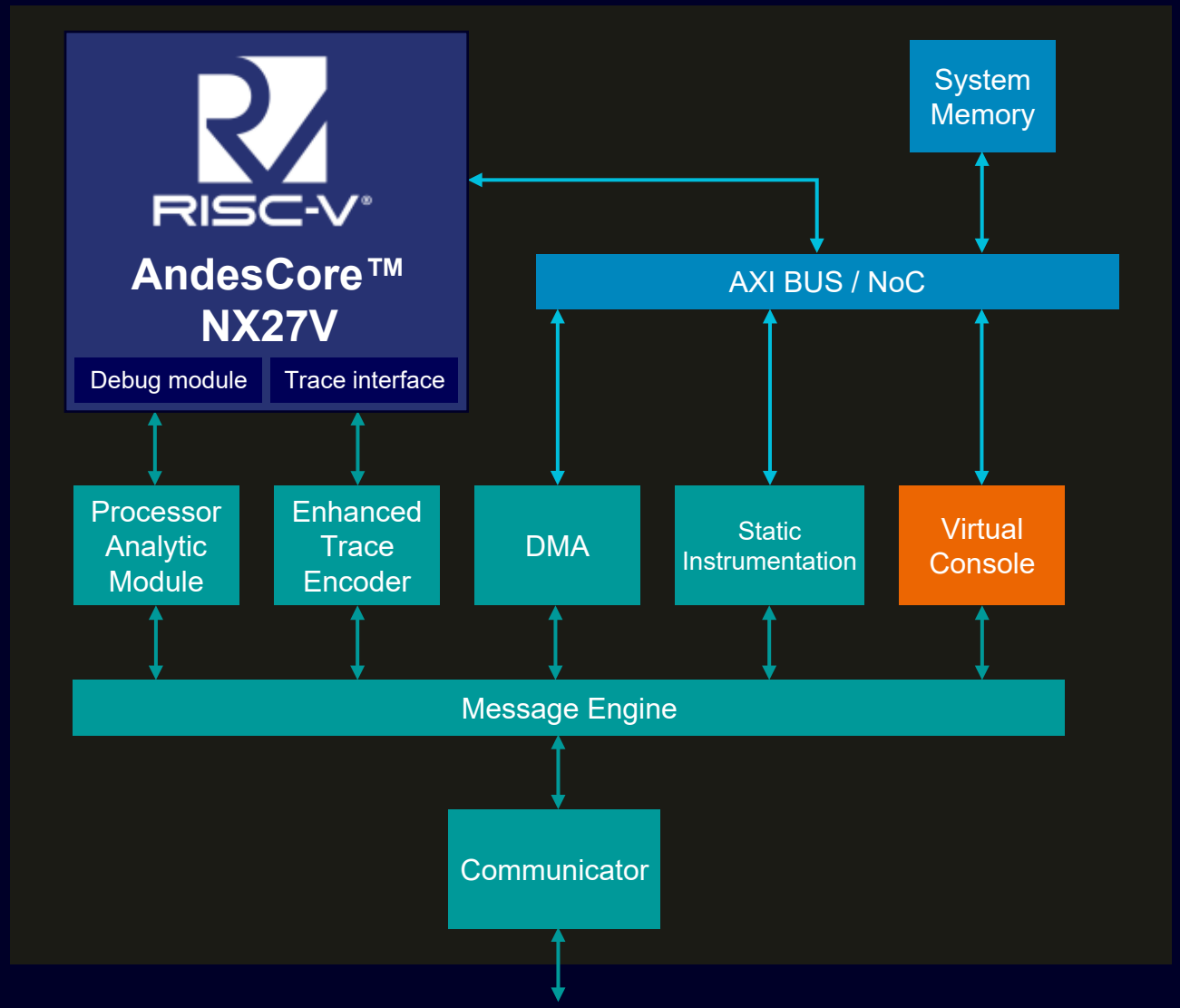
  - Replaces UART interfaces



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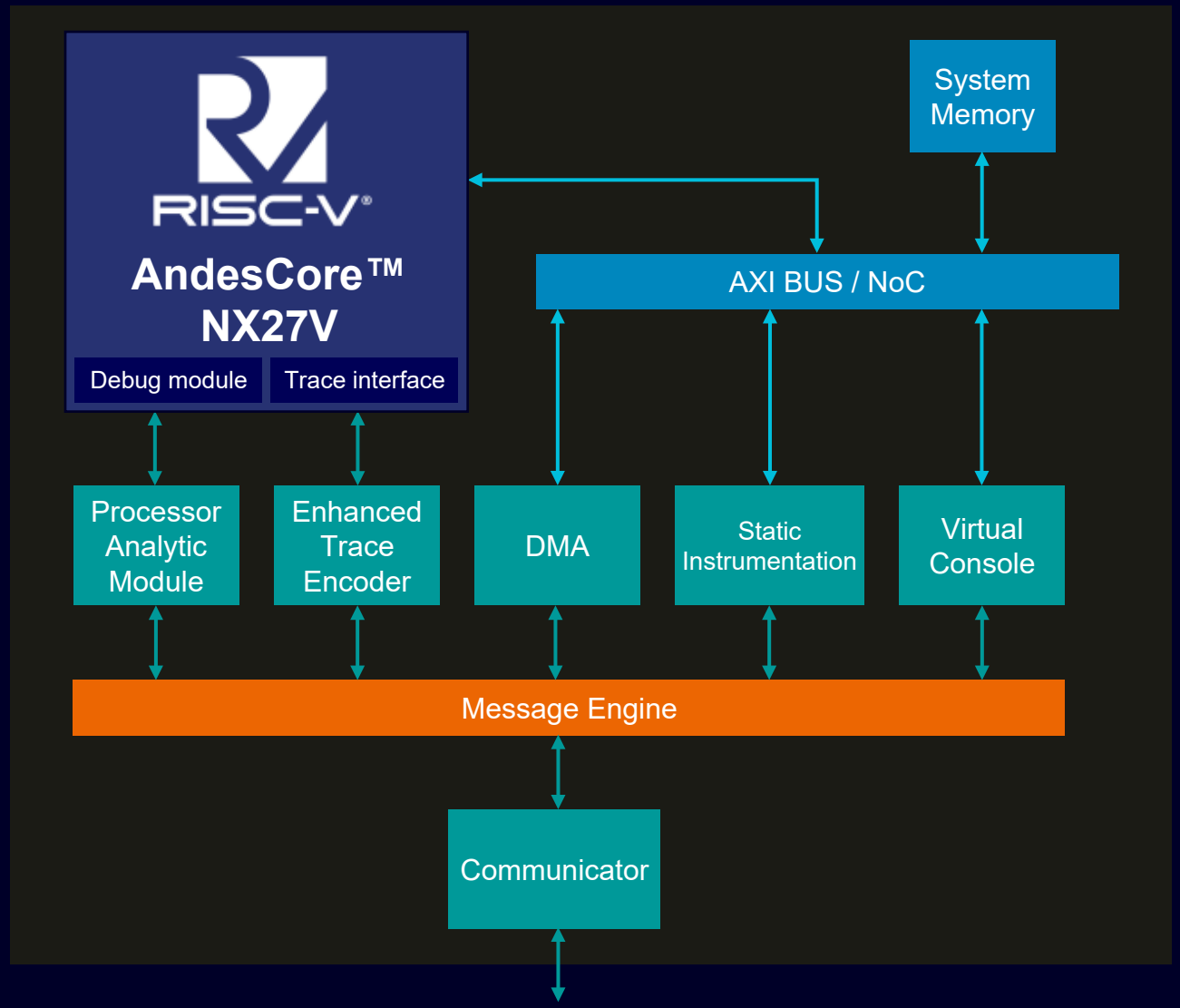
- Messaging Engine
  - Scalable solution



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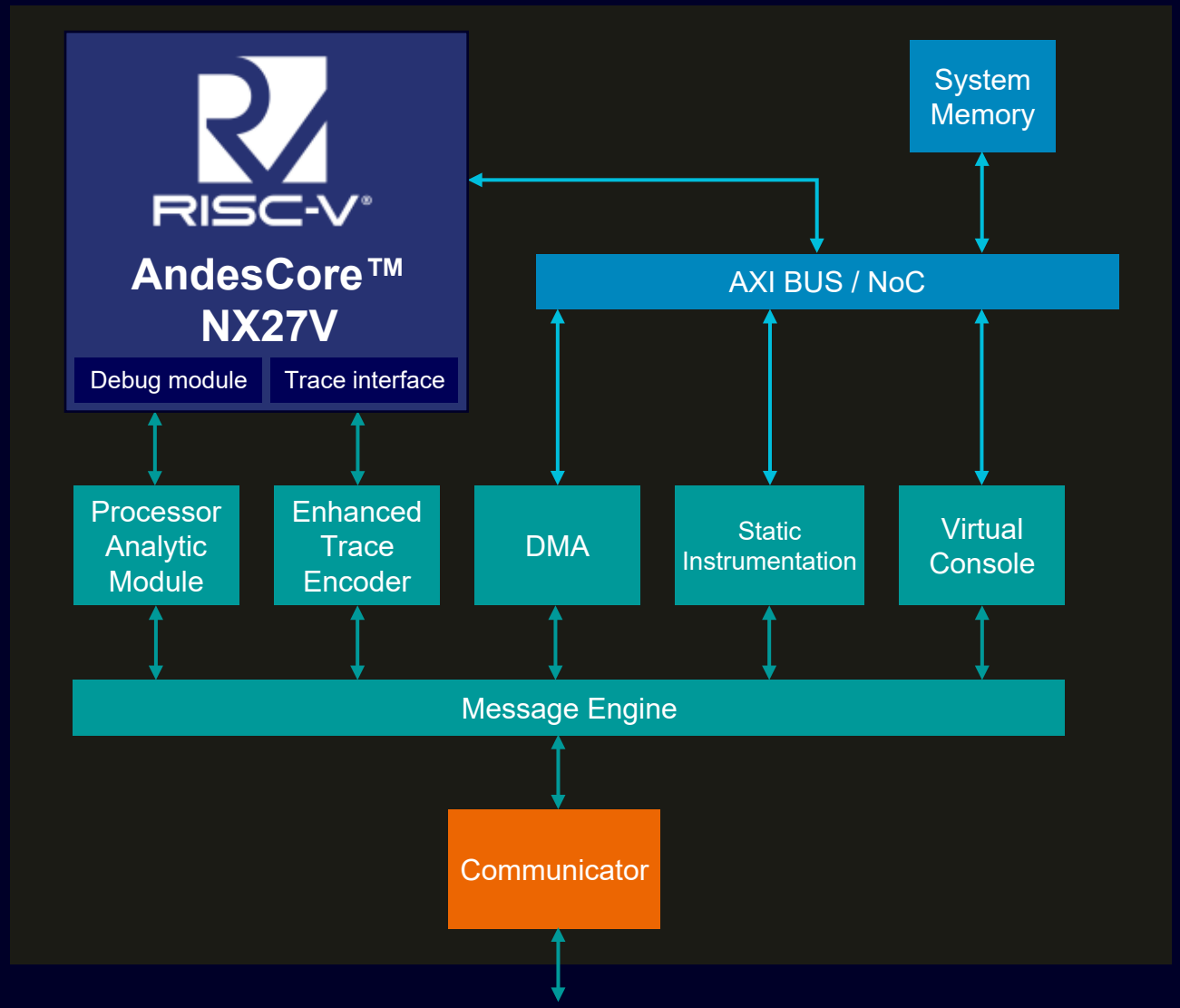
- Communicators
  - Supports USB/JTAG/AXI (for PCIe)



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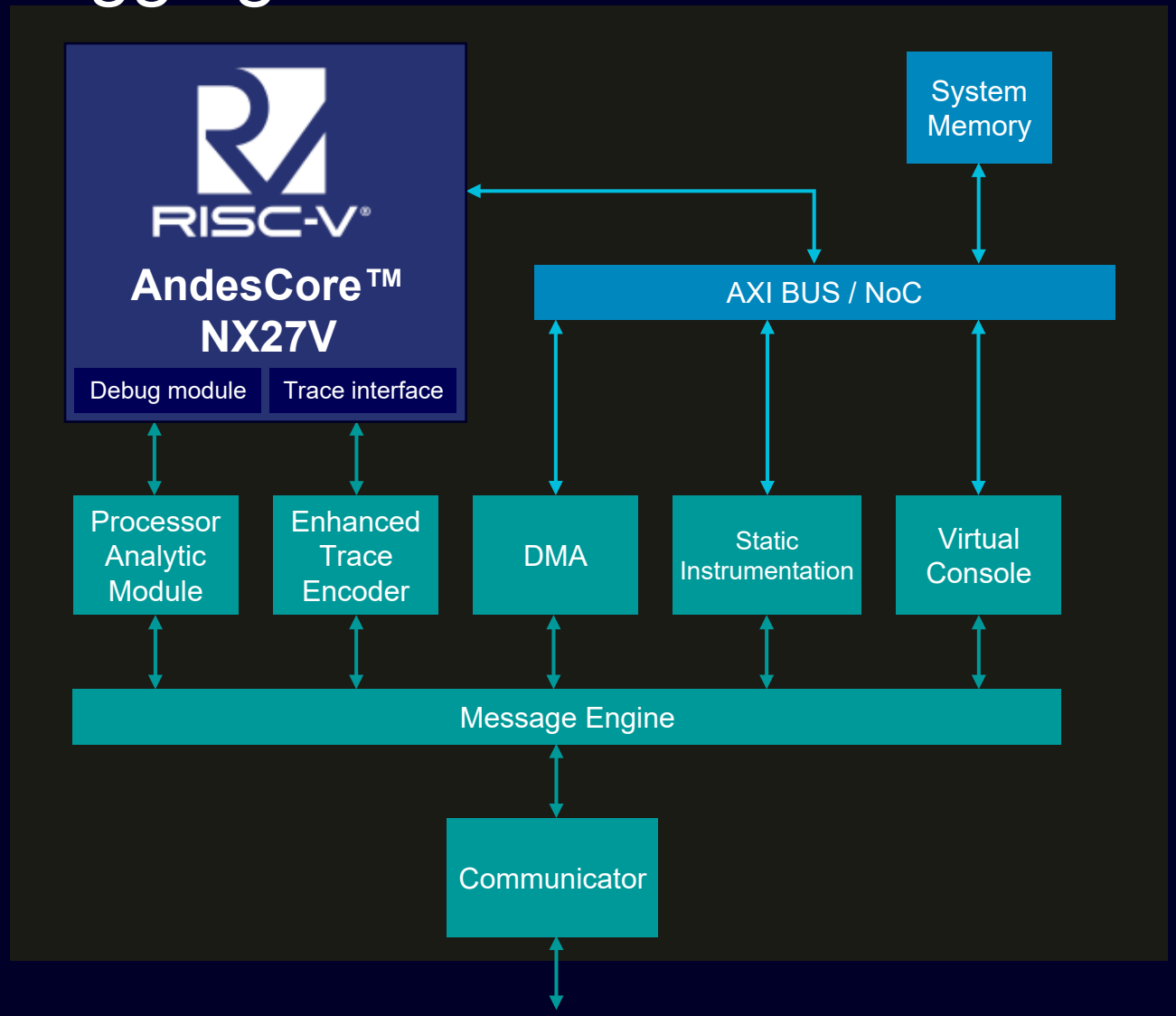

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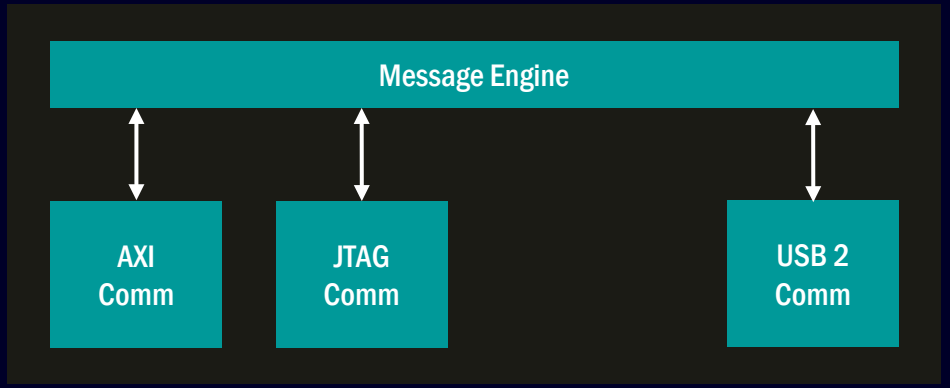
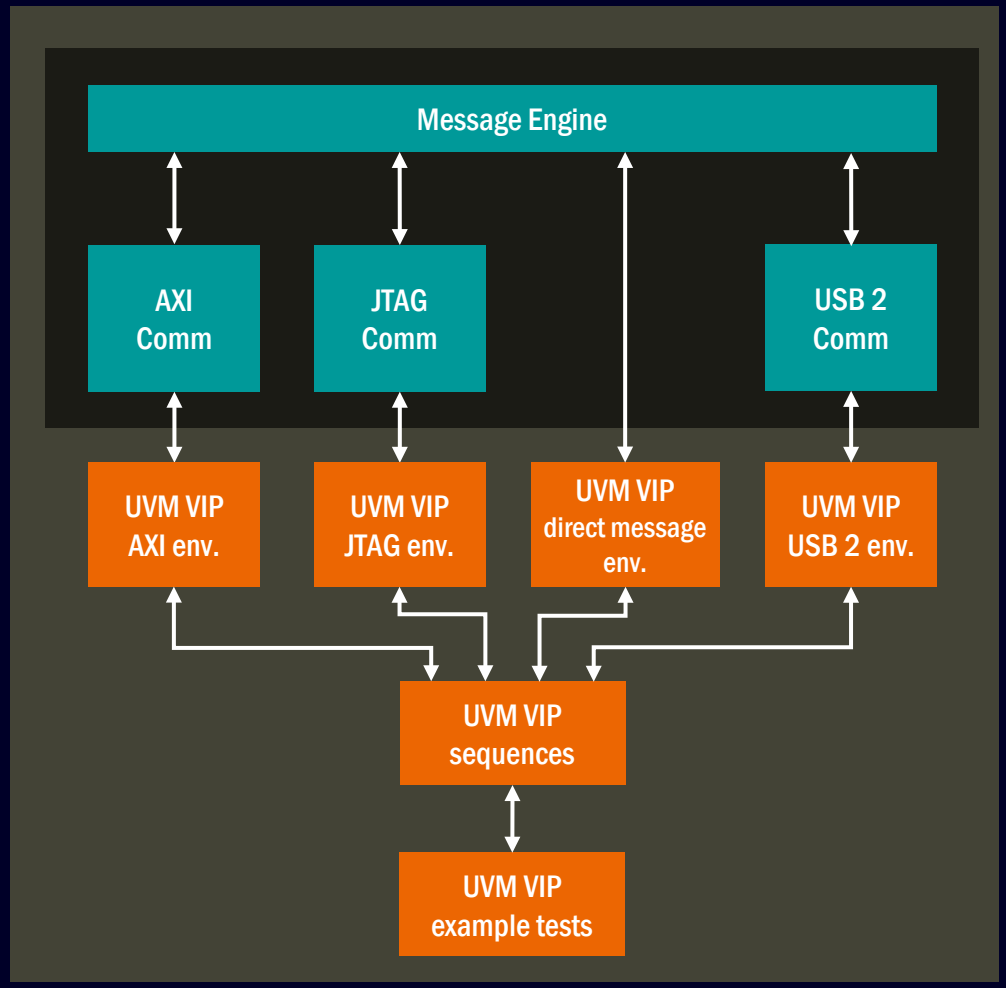
UVM Verification IPs



UVM Verification IPs

- Verifies that UltraSight-V hardware IPs are correctly connected to each other and the SoC components
- UVM integration environment
- Virtual interfaces for each communicator IP
- Example test benches



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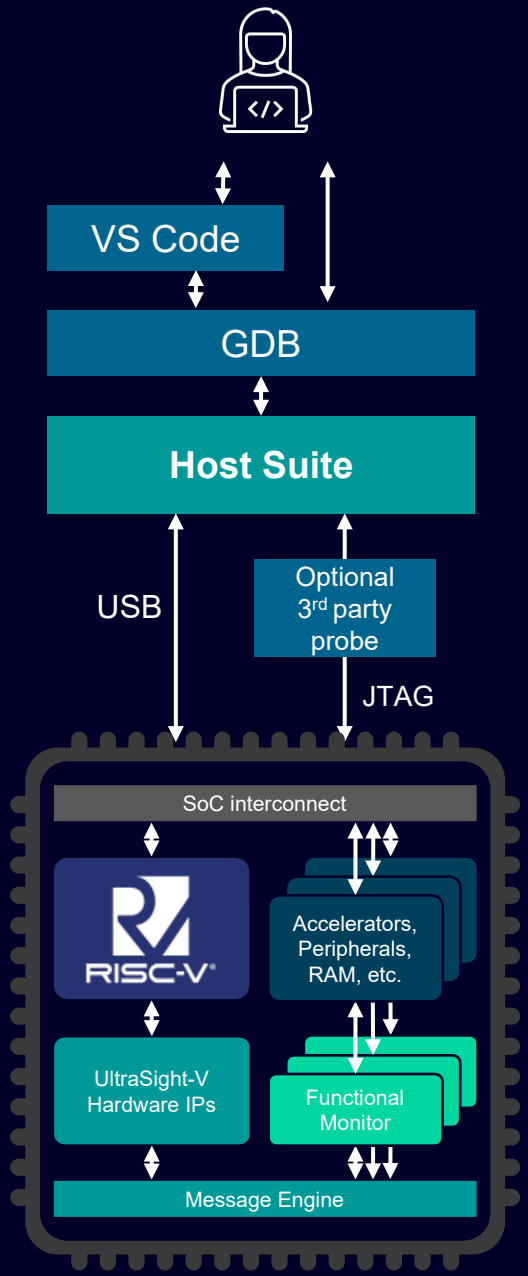
Software Environment

- Runtime control and trace using GDB and OpenOCD
- Integration with common IDEs (e.g. VS Code, Eclipse) or CLI
- Supports USB, JTAG, and AXI communication interface
- Supports RISC-V extensions and custom instructions



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Run Control and Trace

IDE Support

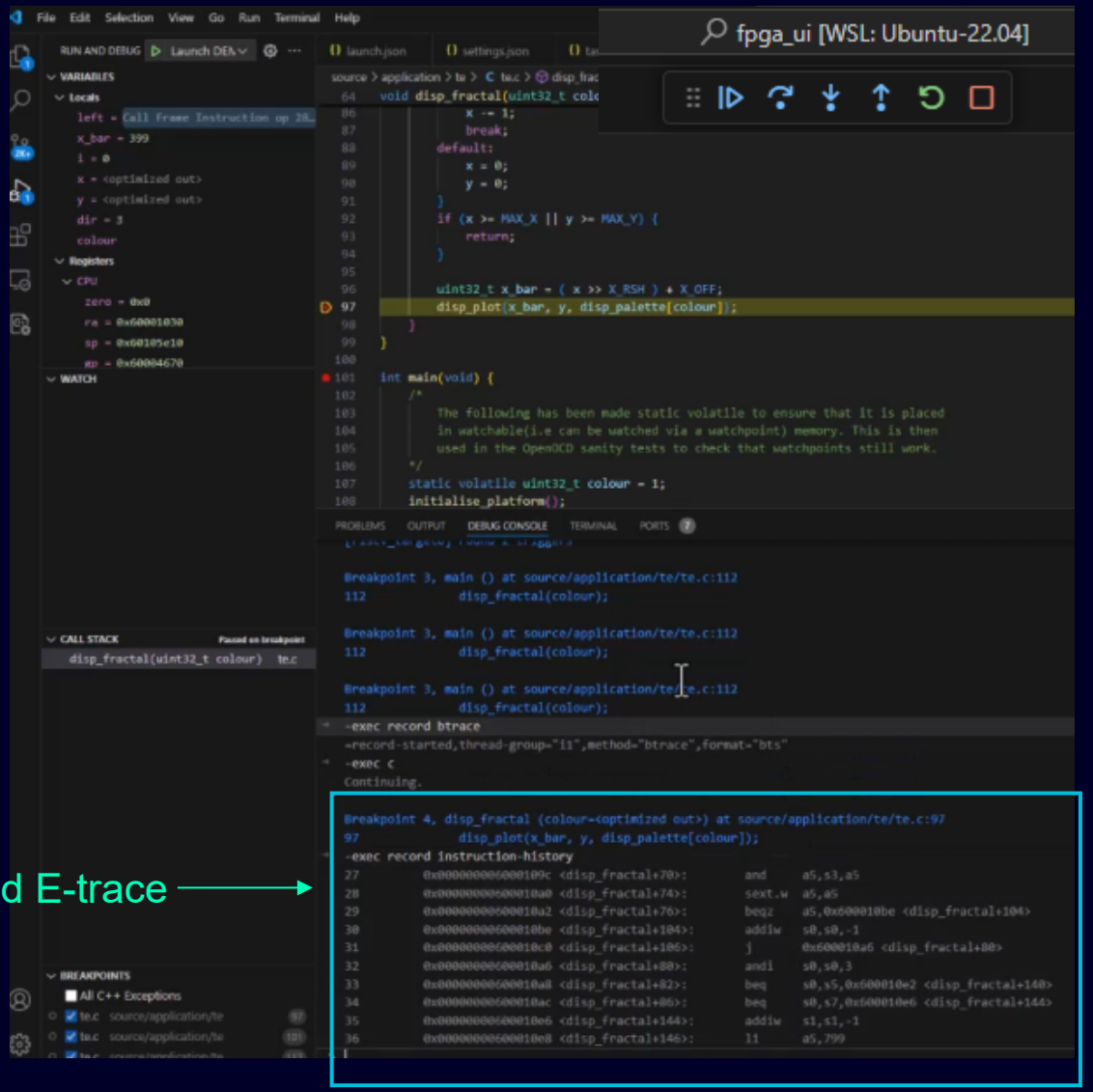
- Compatible with Visual Studio Code

Run-control

- Comprehensive support of RISC-V is enabled through GDB and OpenOCD

E-trace

- Instruction trace reconstruction to ASM and C via GDB
- Custom instructions support



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Efficient Debugging Features

Fast code upload – “fast-load”

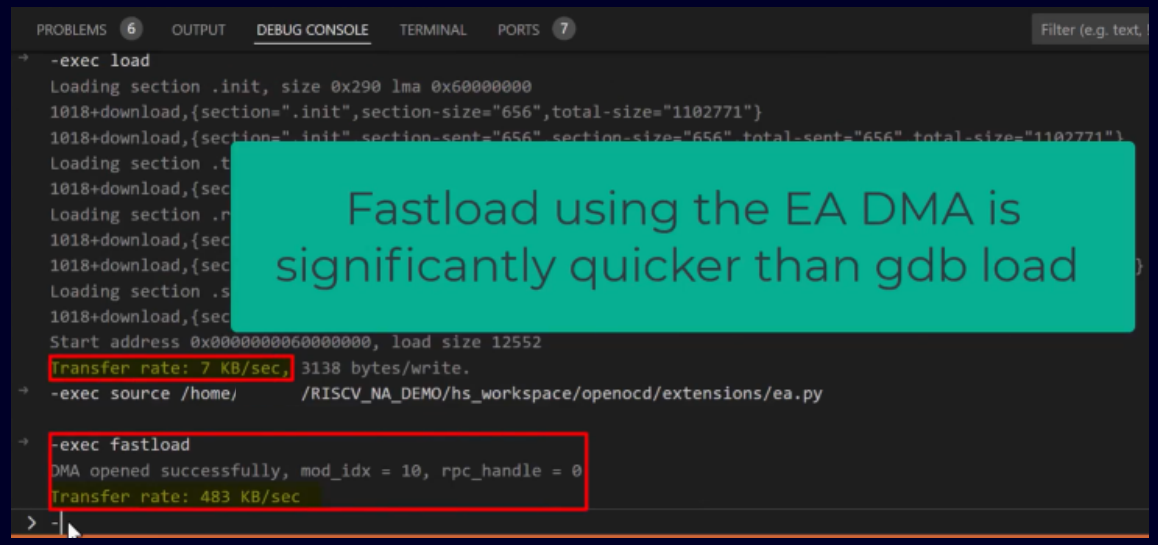
- Uses DMA
- Can be up to 100x faster than normal GDB load

Minimal overhead logging

- printf style debugging with timestamps
- Can take as little as a few instructions (compared to printf at hundreds instructions)

Virtual Console

- Interact with embedded software using UART-like capabilities (e.g. telnet)



Instrument code with printf-style logging macros

```
static void setup( void )
{
    USR_FUNCTION_ENTRY( setup );
    USR_LOGGING_INFO_STRING( "start me up" );
```

```
        smb_write_count_gap = 0;
        UST_LOGGING_DEBUG_PARAM3( "Pixel write y=%d, x=%d, colour=%u", y, x, colour );
```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End-to-end RISC-V Debug and Trace Solution

Scalable to System-wide Debug

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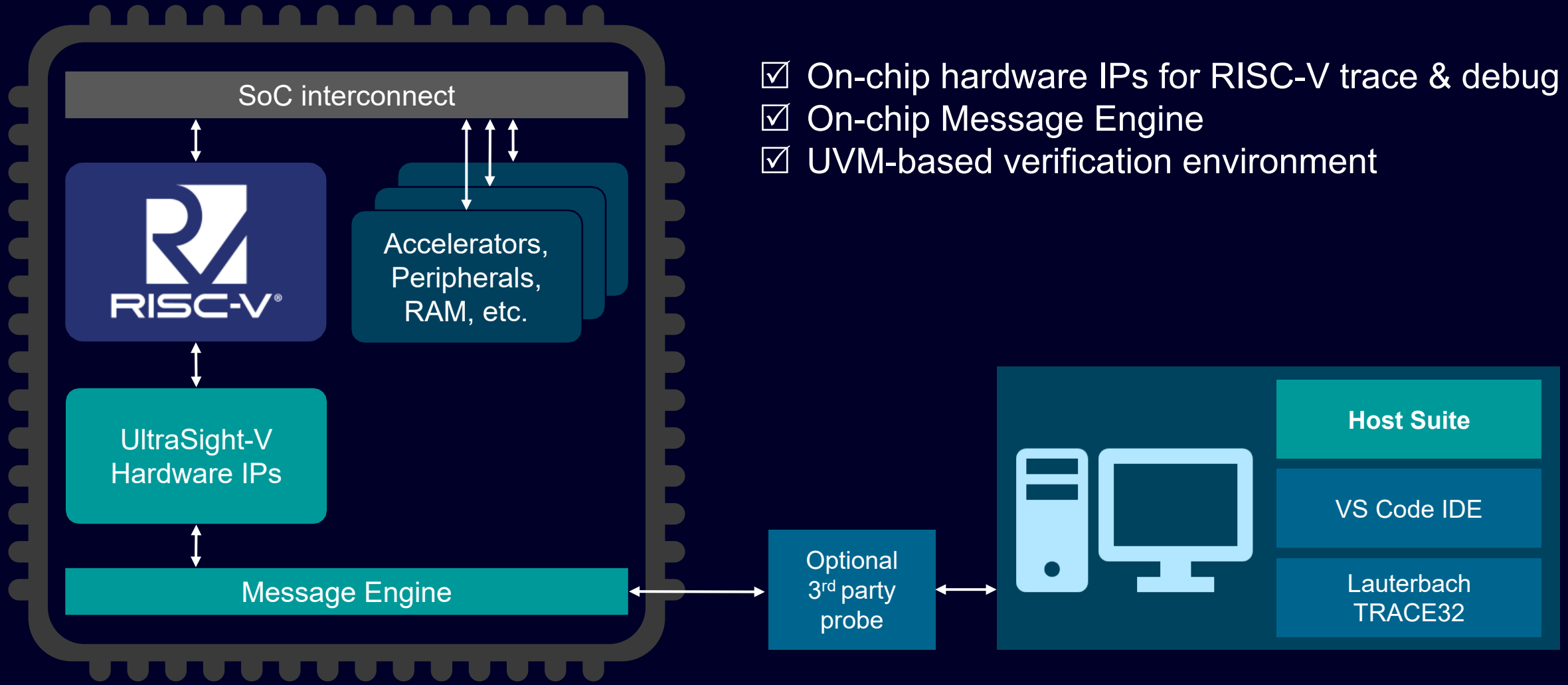
Scalable to full system debug



- ☑ On-chip hardware IPs for RISC-V trace & debug
- ☑ On-chip Message Engine
- ☑ UVM-based verification environment

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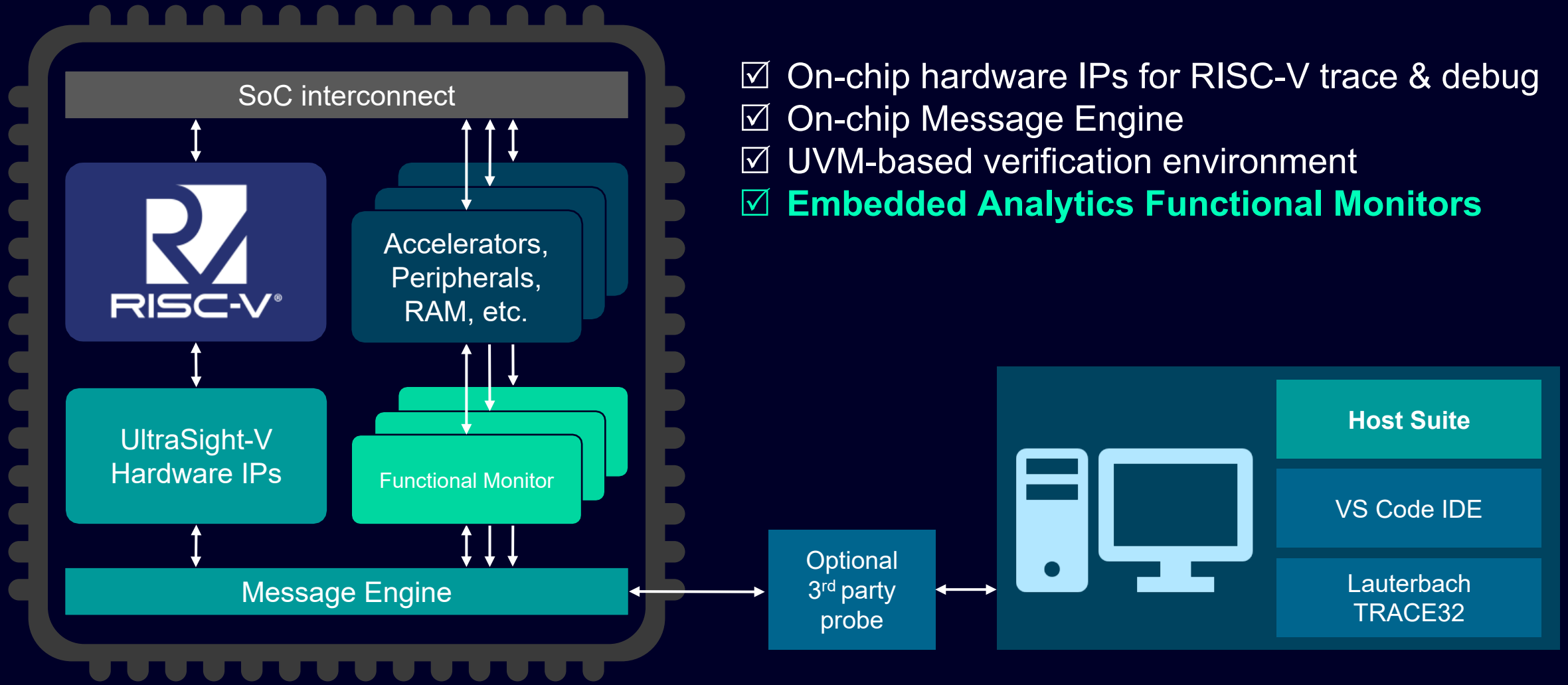
Scalable to full system debug



- ☑ On-chip hardware IPs for RISC-V trace & debug
- ☑ On-chip Message Engine
- ☑ UVM-based verification environment
- ☑ **Embedded Analytics Functional Monitors**

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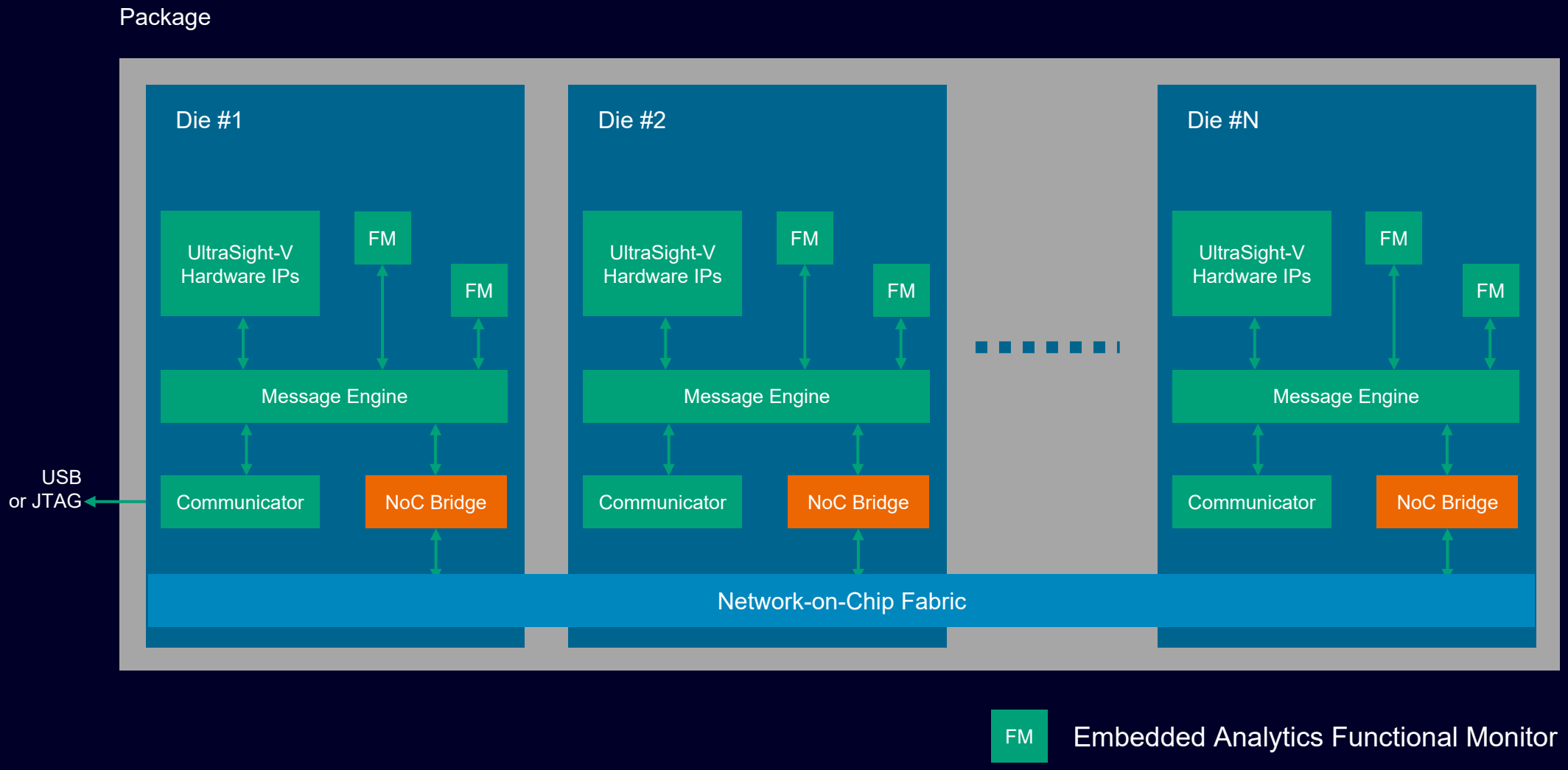
An Example - Scale to Multi-Die Design



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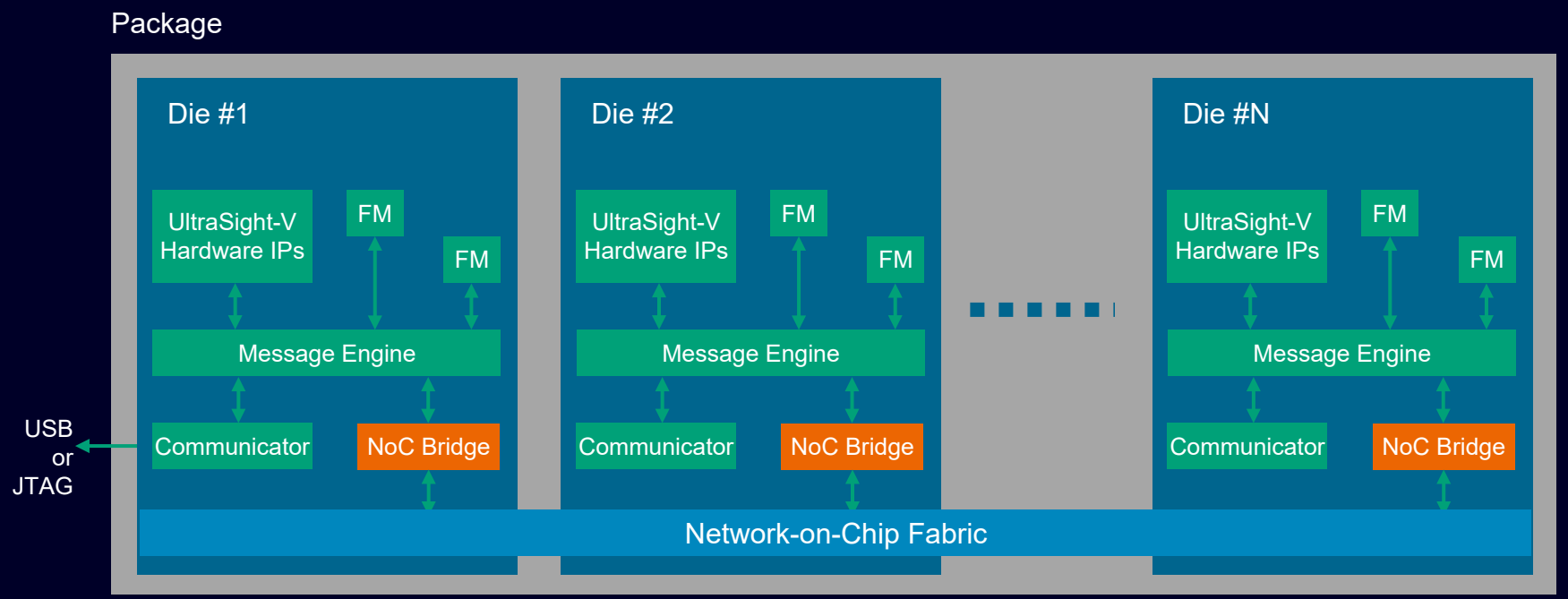
Scale to Multi-Die Design

Extends visibility in multi-die systems



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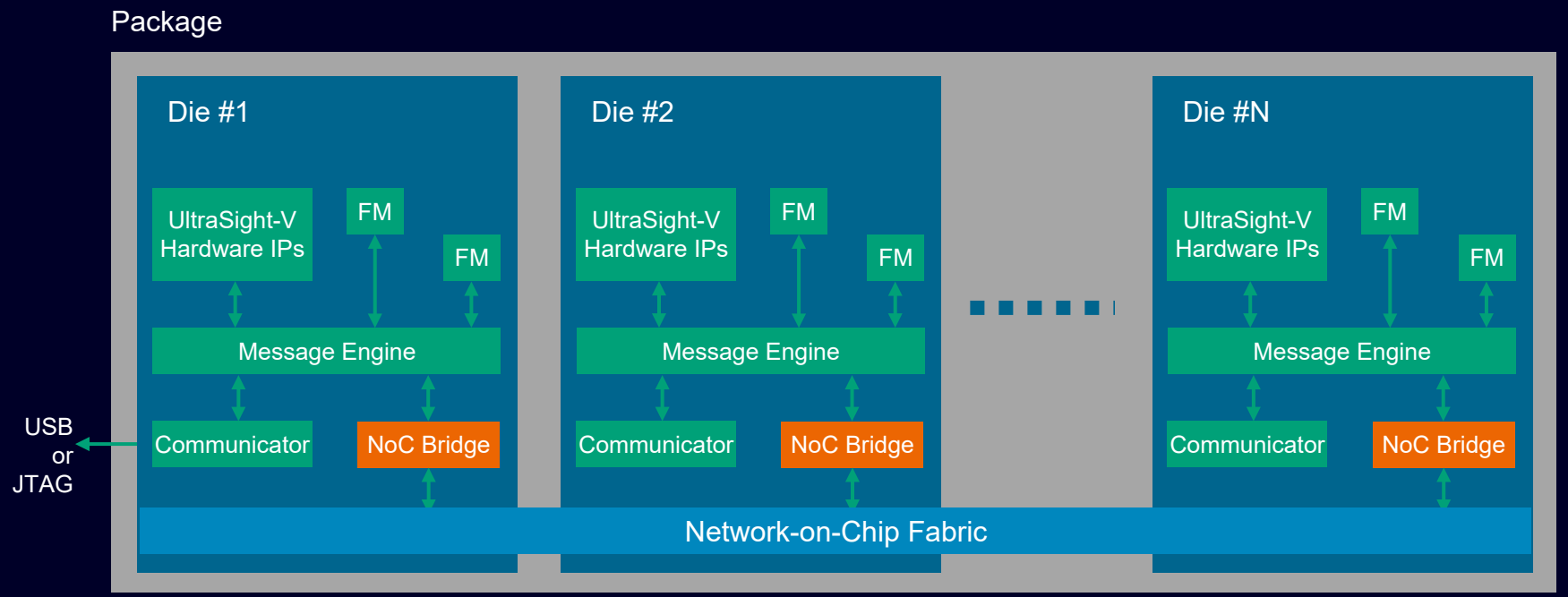
Extends visibility in multi-die systems

Any die can utilize Functional Monitors (FM)



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Scale to Multi-Die Design

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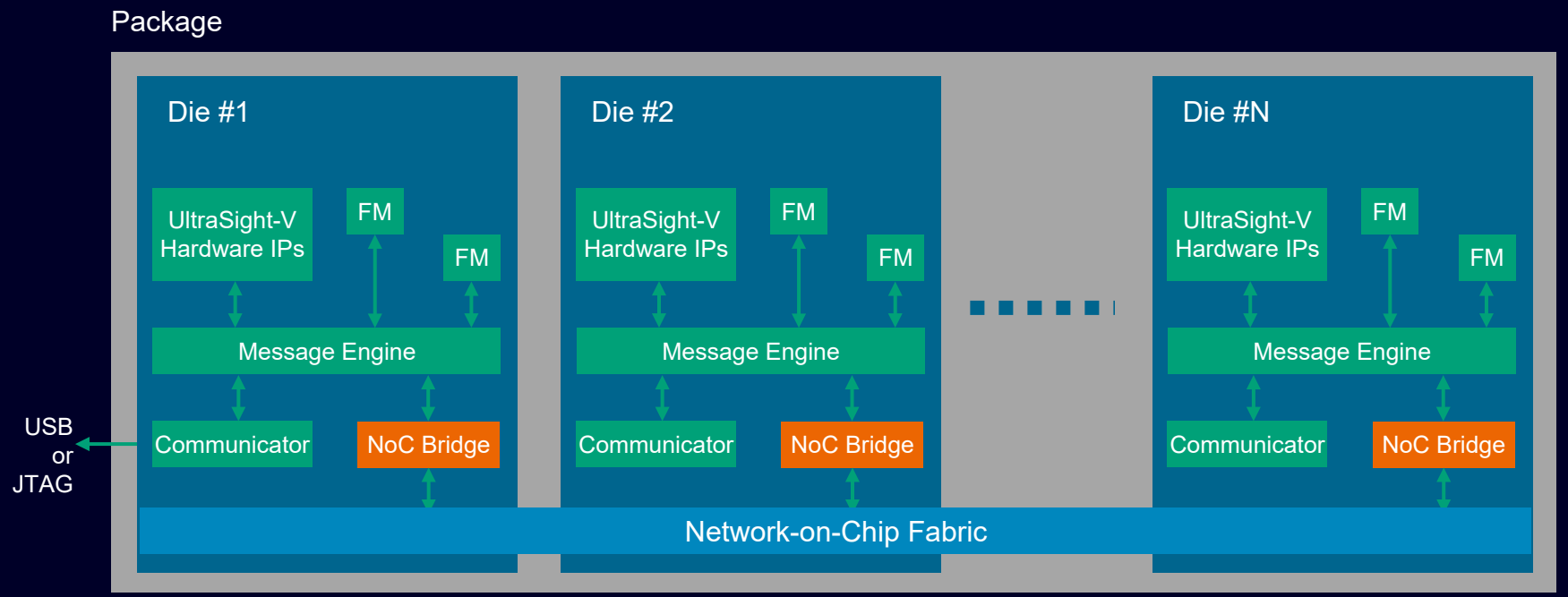
Any die can utilize Functional Monitors (FM)

Methodology proven for multi-die design



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Why Tessent UltraSight-V

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End-to-end RISC-V
Debug & Trace Solution

Reducing your time to market

Code Debug

- Run Control
- Fast memory access
- Instrumentation

Efficient Trace

- Highly-compressed instruction trace (E-trace)

Interface Options

- JTAG
- USB
- AXI (for PCIe access)

Software Toolkit

- Supports VS Code IDE
- UVM Verification IP

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Scalable to System-wide Debug

Enabling you to future-proof your design

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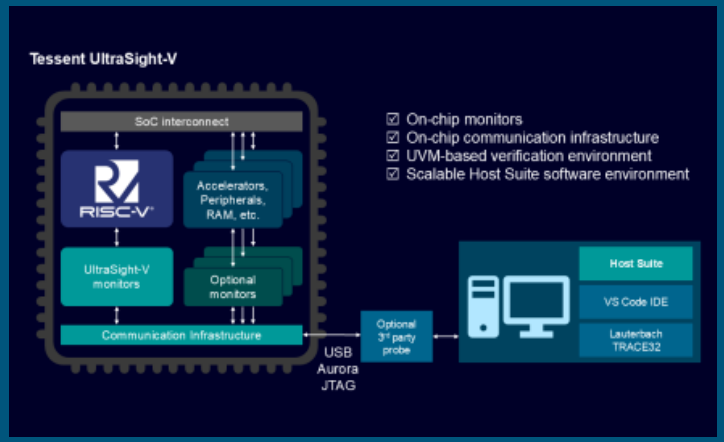
Learn more

www.siemens.com/tessent/embedded-analytics/

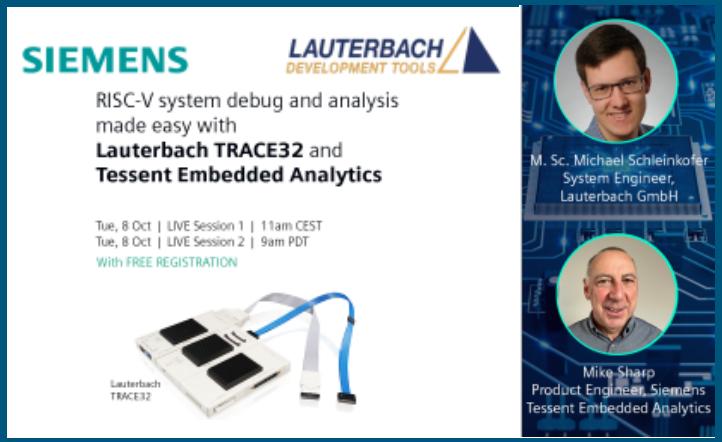
Tessent UltraSight-V

Learn more about the Tessent UltraSight-V solution, factsheet and video demo available



Webinar
RISC-V debug made easy

How Tessent UltraSight-V and Lauterbach TRACE32® work together to simplify RISC-V system debug

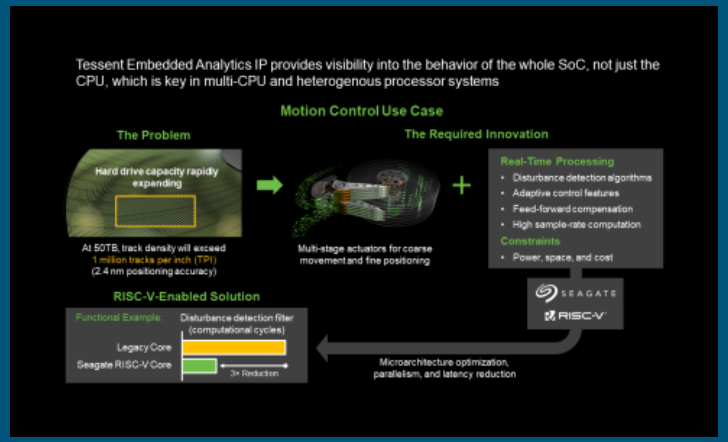


Technical presentation
RISC-V Trace

An overview of the Efficient Trace (E-Trace) standard and how processor trace is used to improve embedded software and applications.

Case study
Seagate

How Seagate Technology use Tessent Embedded Analytics products to improve debug and optimization challenges in their RISC-V SoCs.



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