

# Tessent™ UltraSight-V

An On-chip Debug and Trace Solution for RISC-V  
Systems

Yifan Li, Account Technology Manager

Tessent Products

Siemens EDA

# Traditional SoC Debug Needs Help

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debug  
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- Silent data corruption



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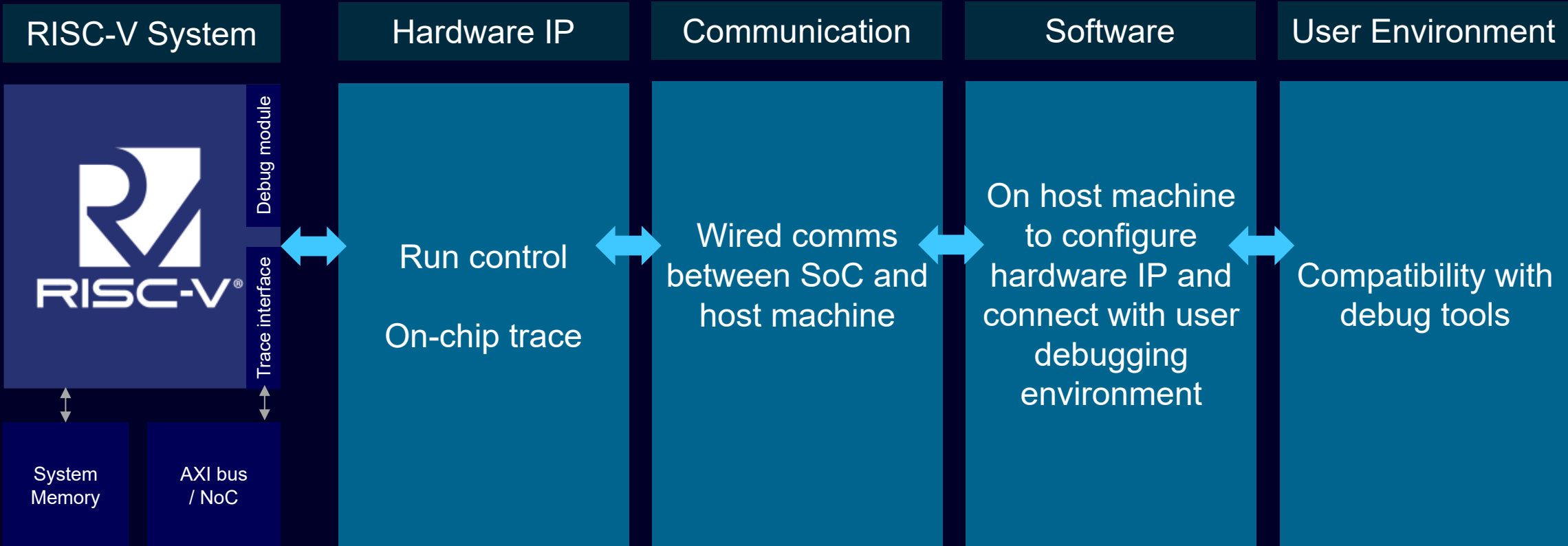
- Software complexity
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**Identifying hardware and real-time software issues require more efficient methods to observe, to debug, to iterate, and to scale**



Low  
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productivity

# Growing Markets Demand Scalable Debug Solution



# Growing Markets Demand Pre-verified IP Solution

~50%

Mean ASIC project time spent  
in verification

*“Projects spending minimal time typically reuse pre-verified IP modules, reducing verification overhead.”*

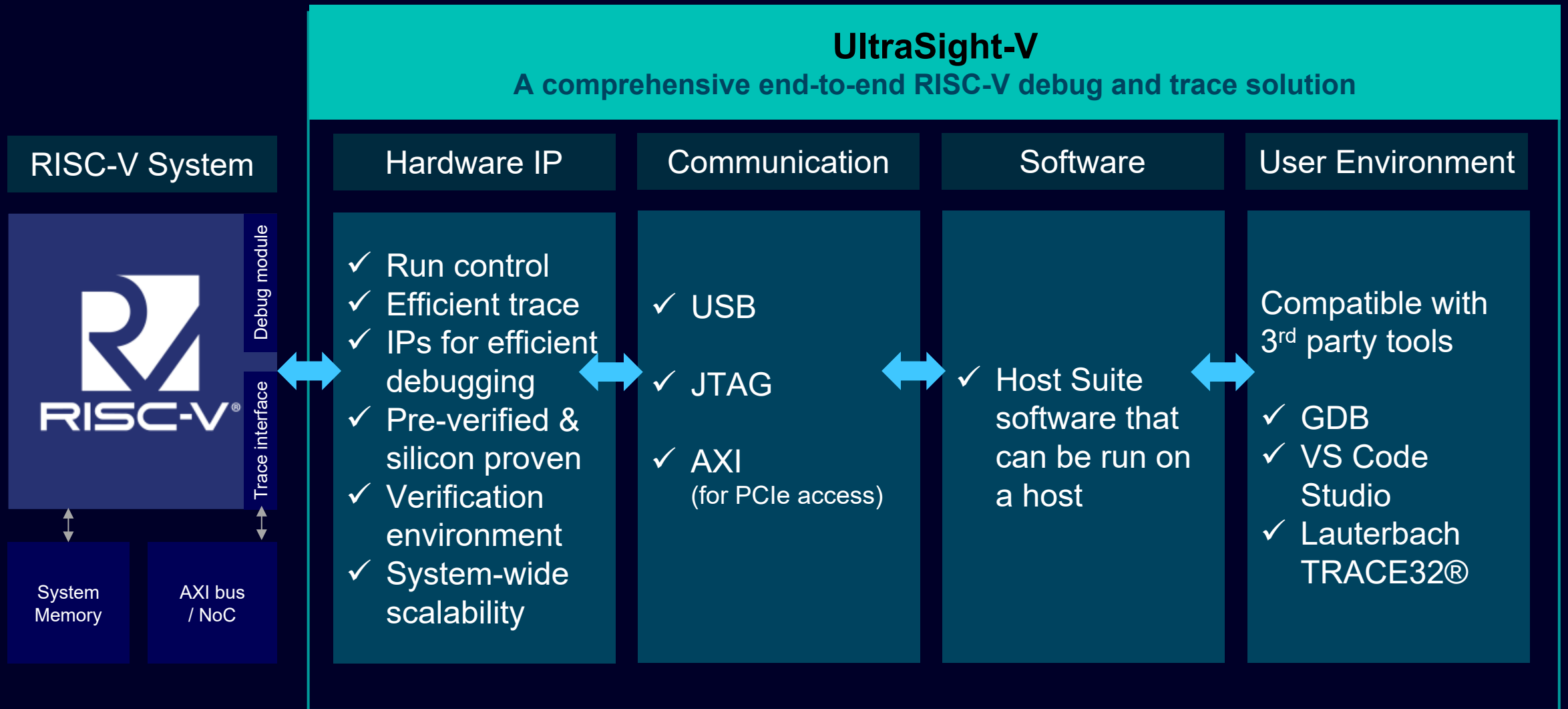
*“Conversely, projects with significant verification time often involve high proportions of newly developed IP”*

*By 2024 Wilson Research Group IC/ASIC functional verification trend report*

# End-to-end RISC-V Debug & Trace Solution

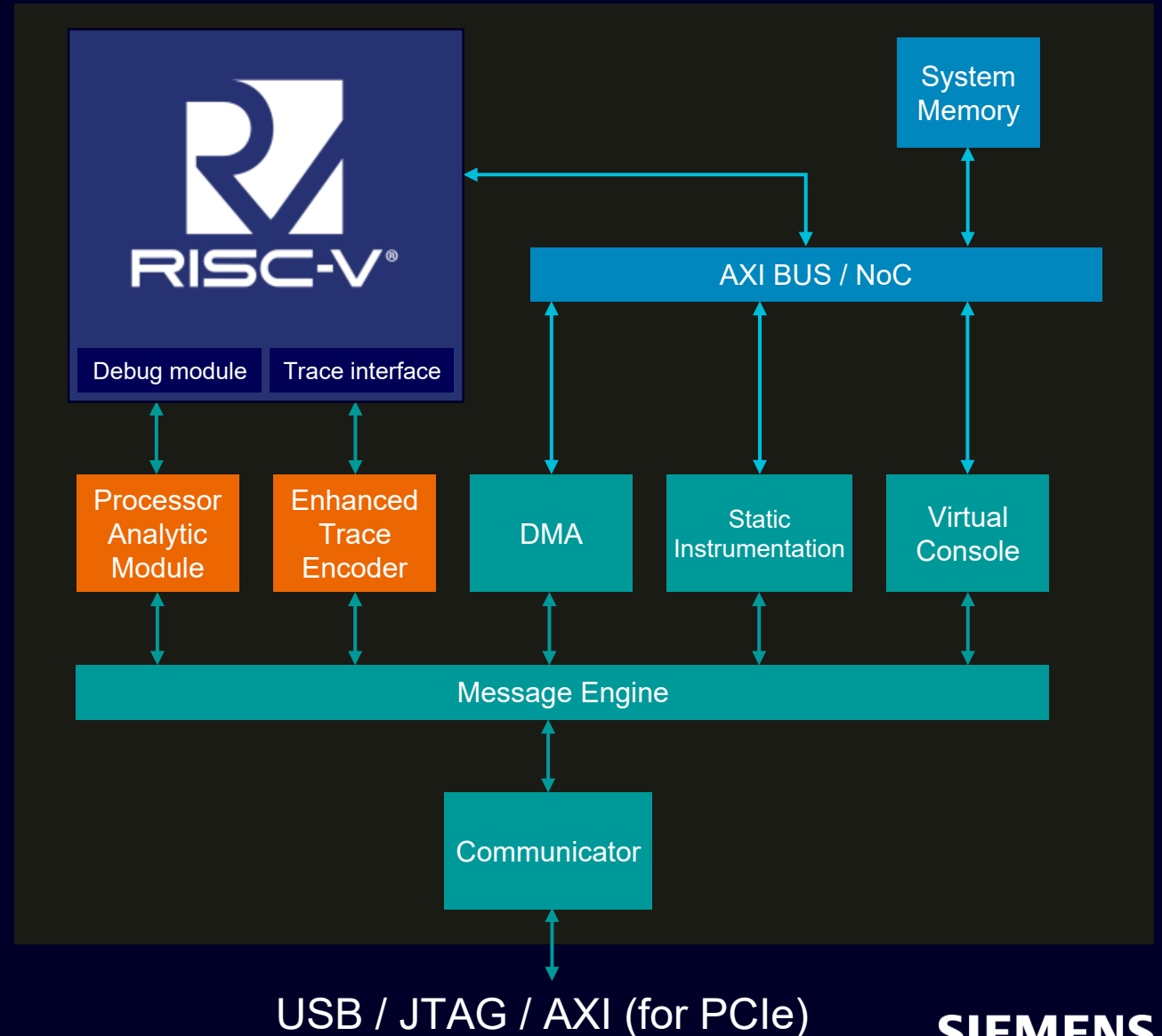
Scalable to  
System-wide Debug

# Tessent UltraSight-V



# Hardware IPs to Debug RISC-V Cores

- Processor Analytic Module
  - Provides run control capabilities
- Enhanced Trace Encoder
  - Outputs processor trace (**E-Trace**)



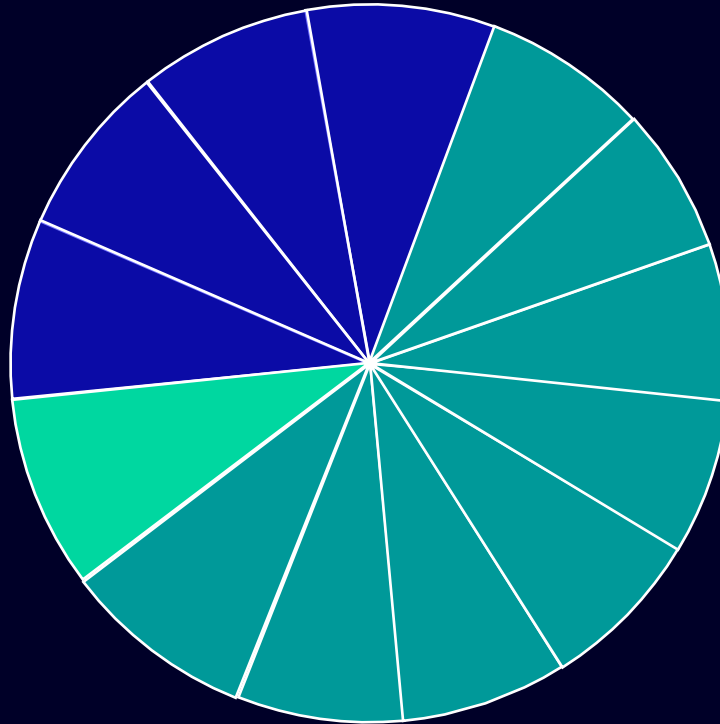
# Enhanced Trace Encoder IP

## RISC-V Trace mandatory features

- Instruction trace
- Hart to encoder interface
- 'Delta Address' trace mode
- Efficient packet format

## Tessent Embedded Analytics

- Cycle accurate trace



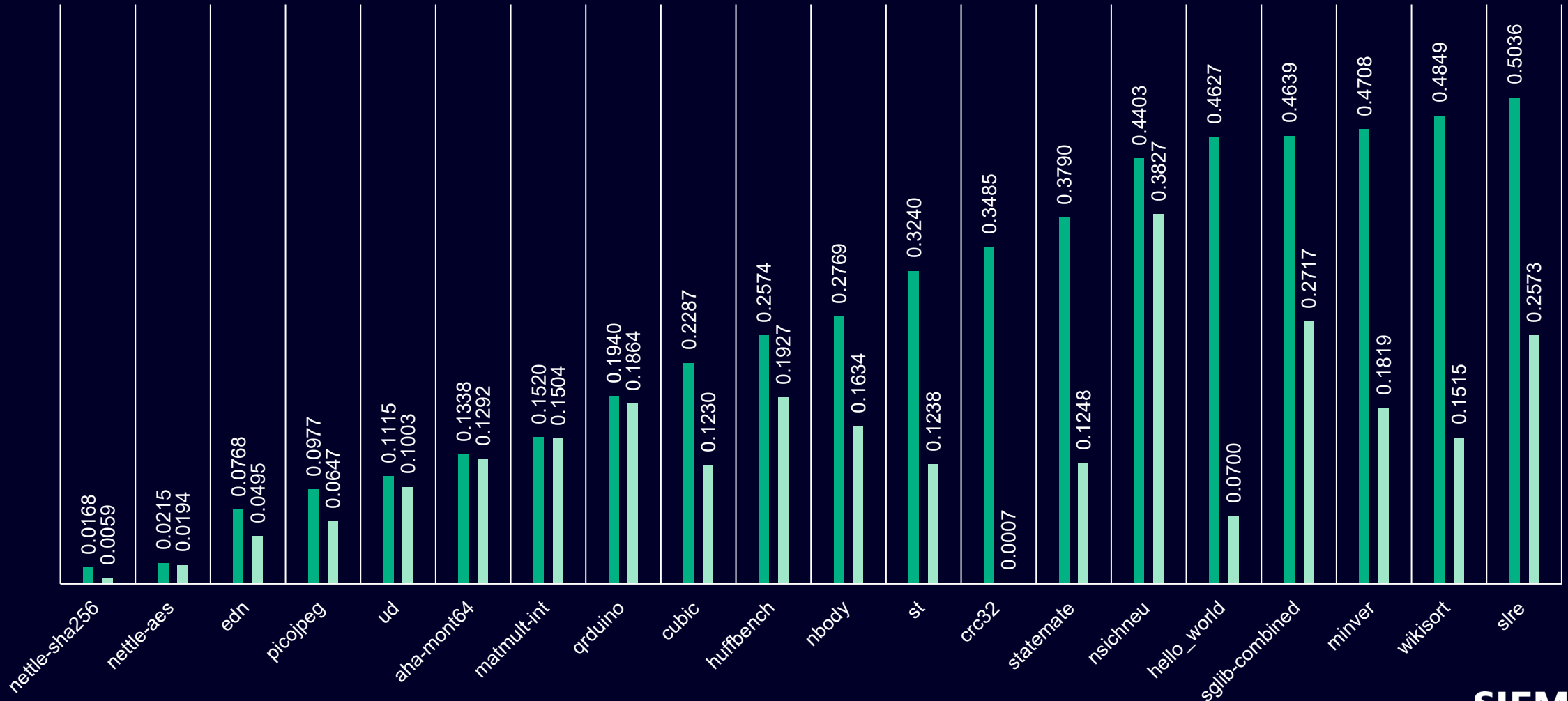
## RISC-V Trace optional extensions

- Multiple instruction retirement
- Sequentially inferable jump mode
- Implicit return mode
- Branch Prediction mode
- Jump Target Cache mode
- Full Address mode
- Sign-based compression
- Filtering

# Trace Compression - Embench™ Benchmark Results

~40% BPI improvement with optional extensions

■ BPI No extensions ■ BPI With Extensions

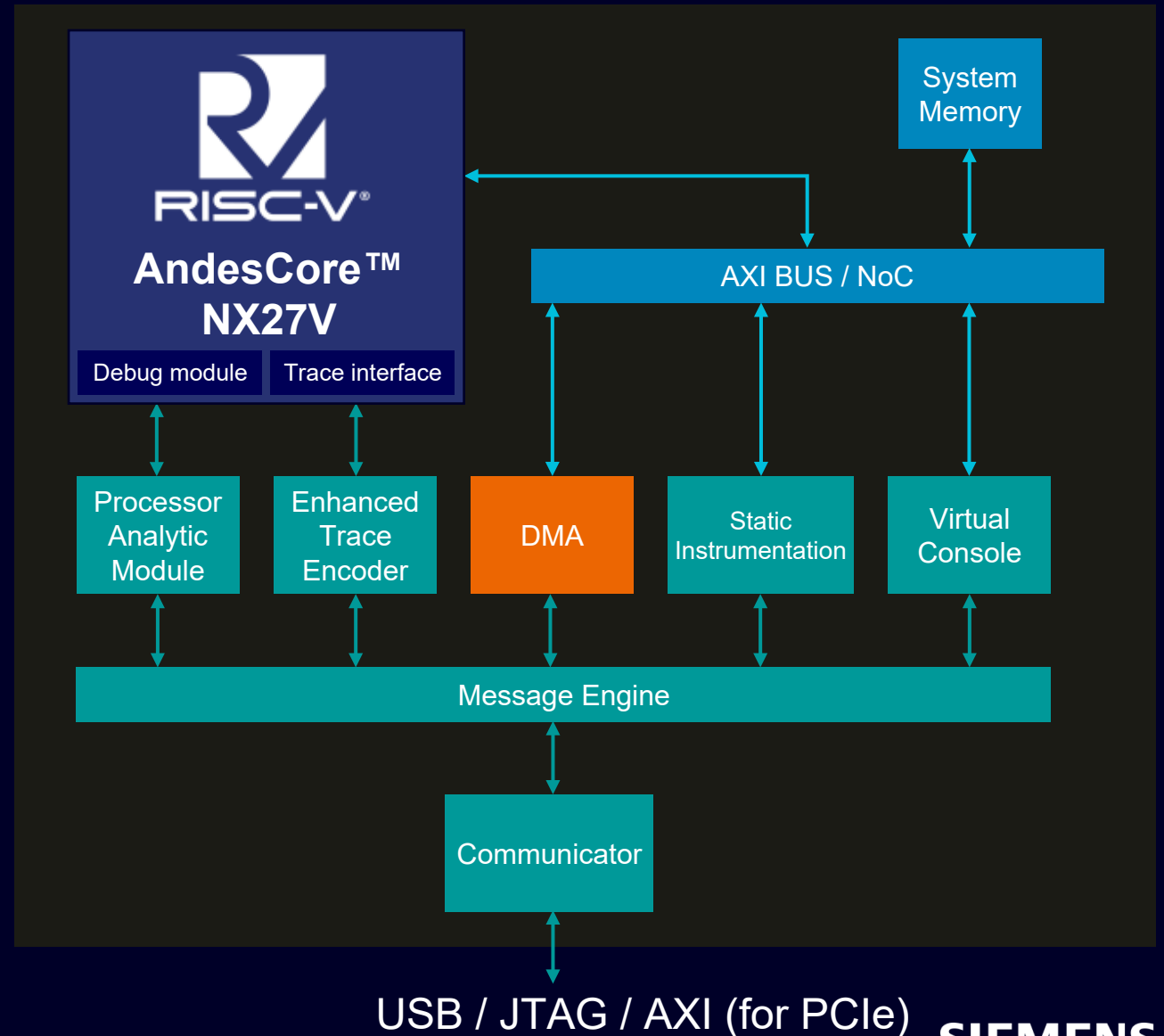


# Hardware IPs for Efficient Debugging

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## Hardware IPs (Parametrized RTL)

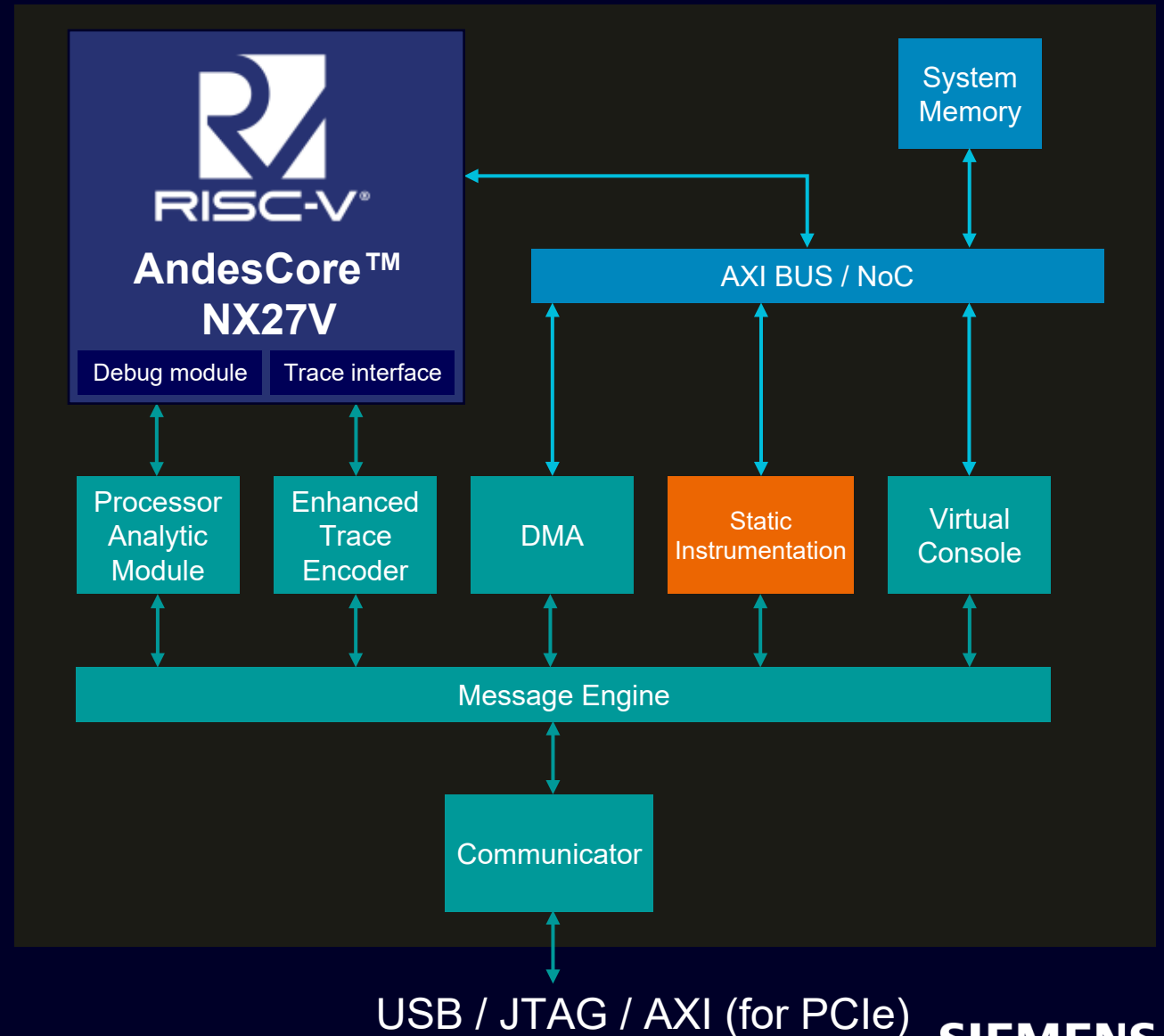
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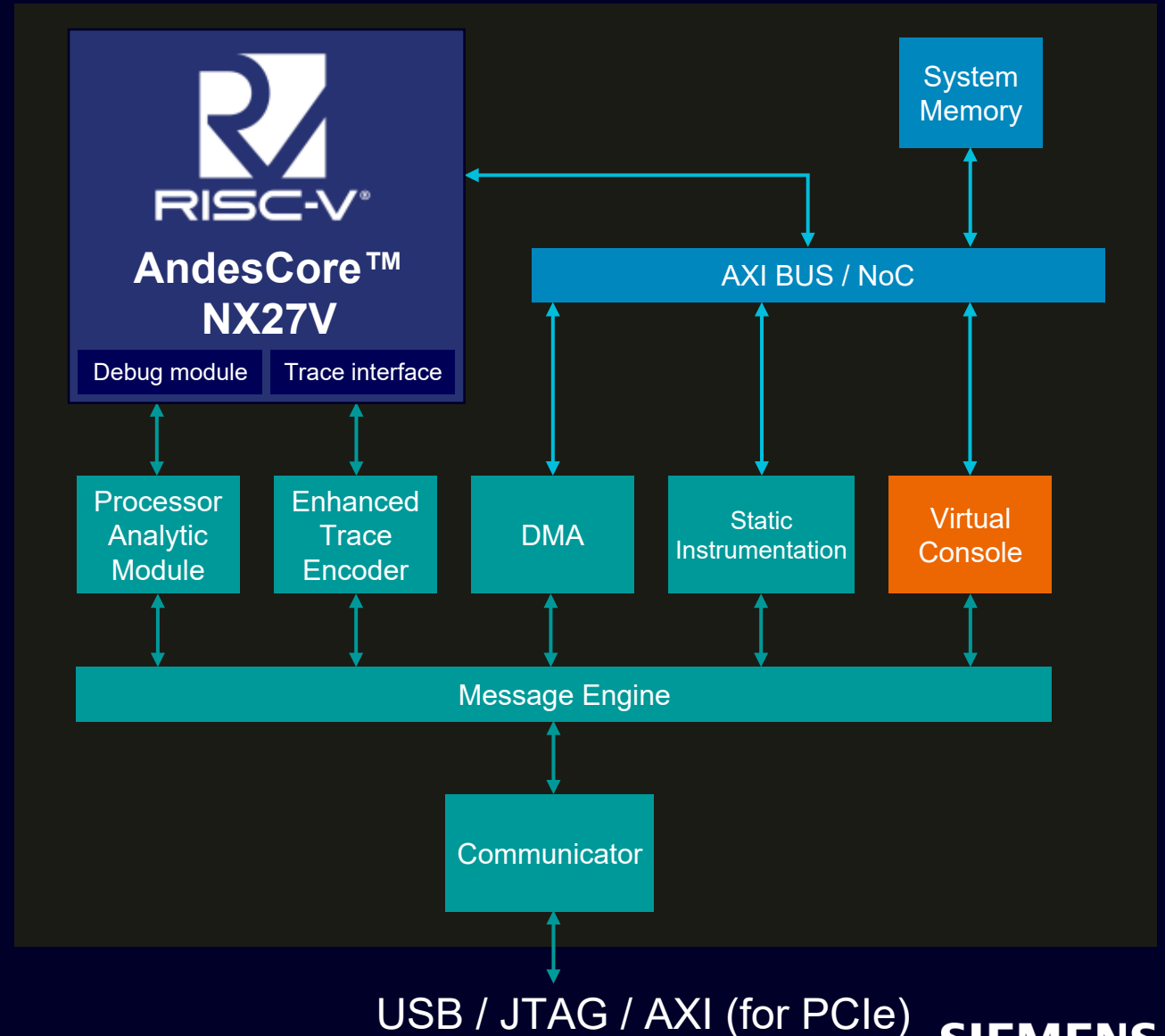
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  - Minimally invasive logging



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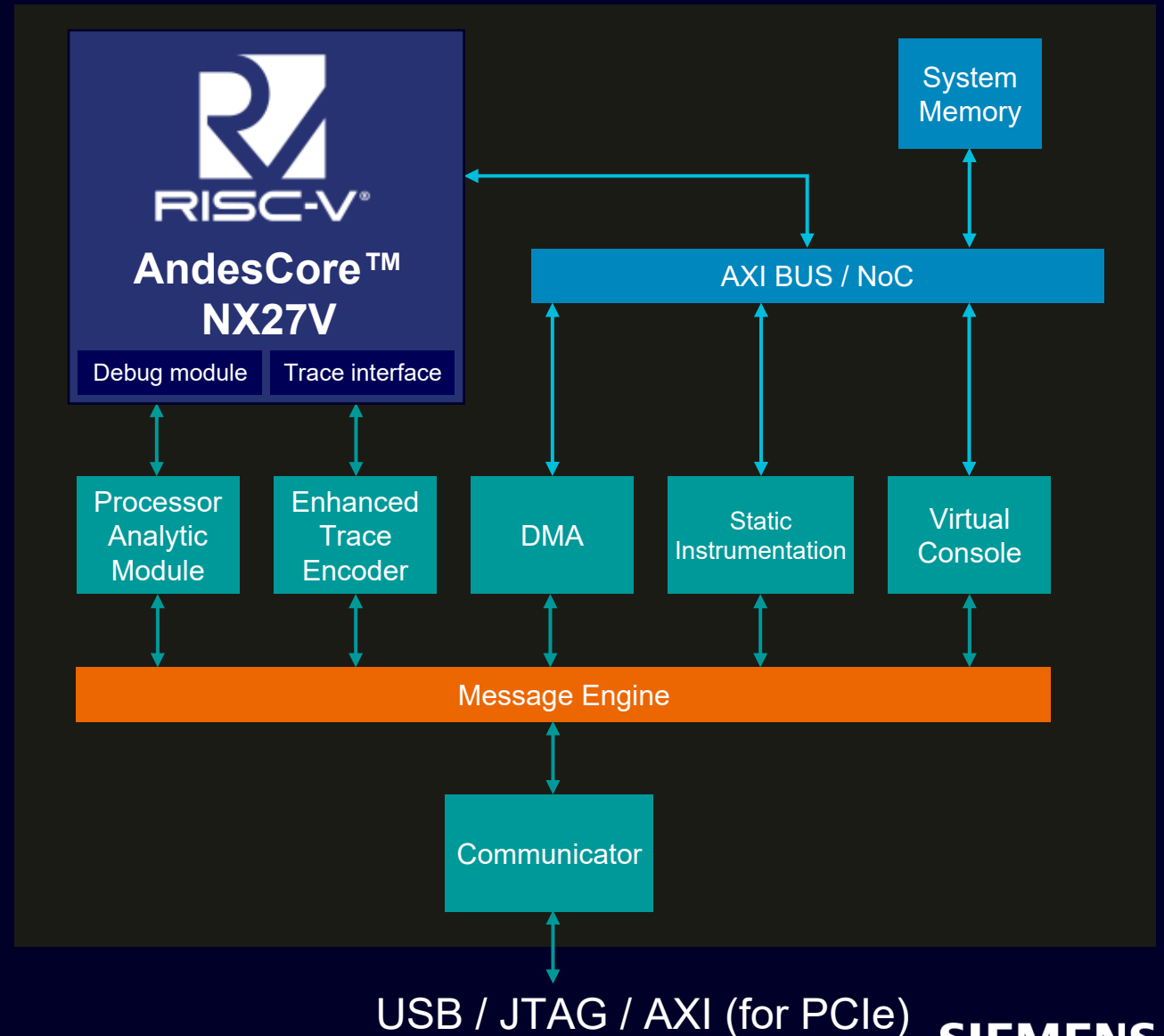
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- Virtual console
  - Replaces UART interfaces



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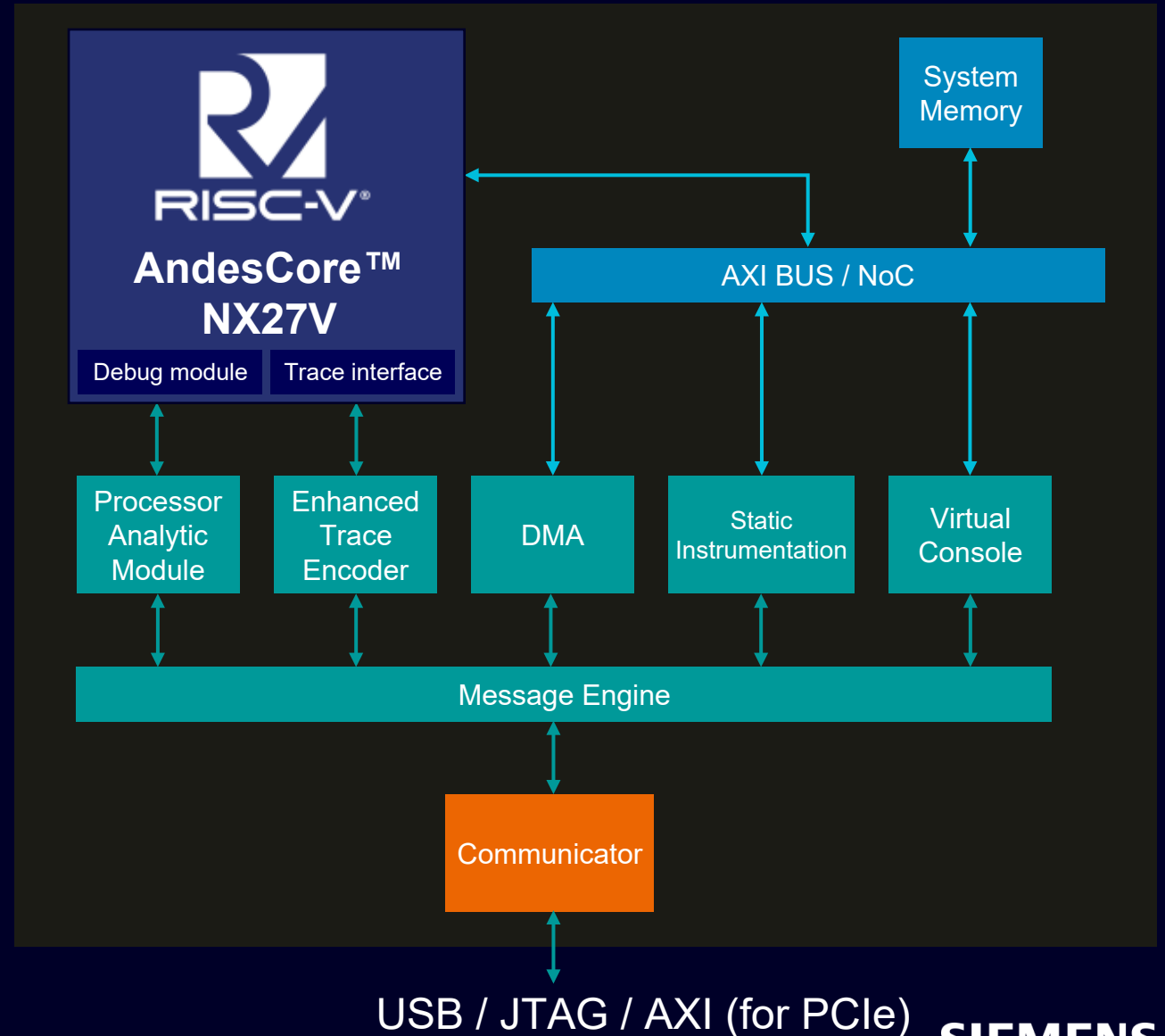
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- Messaging Engine
  - Scalable solution



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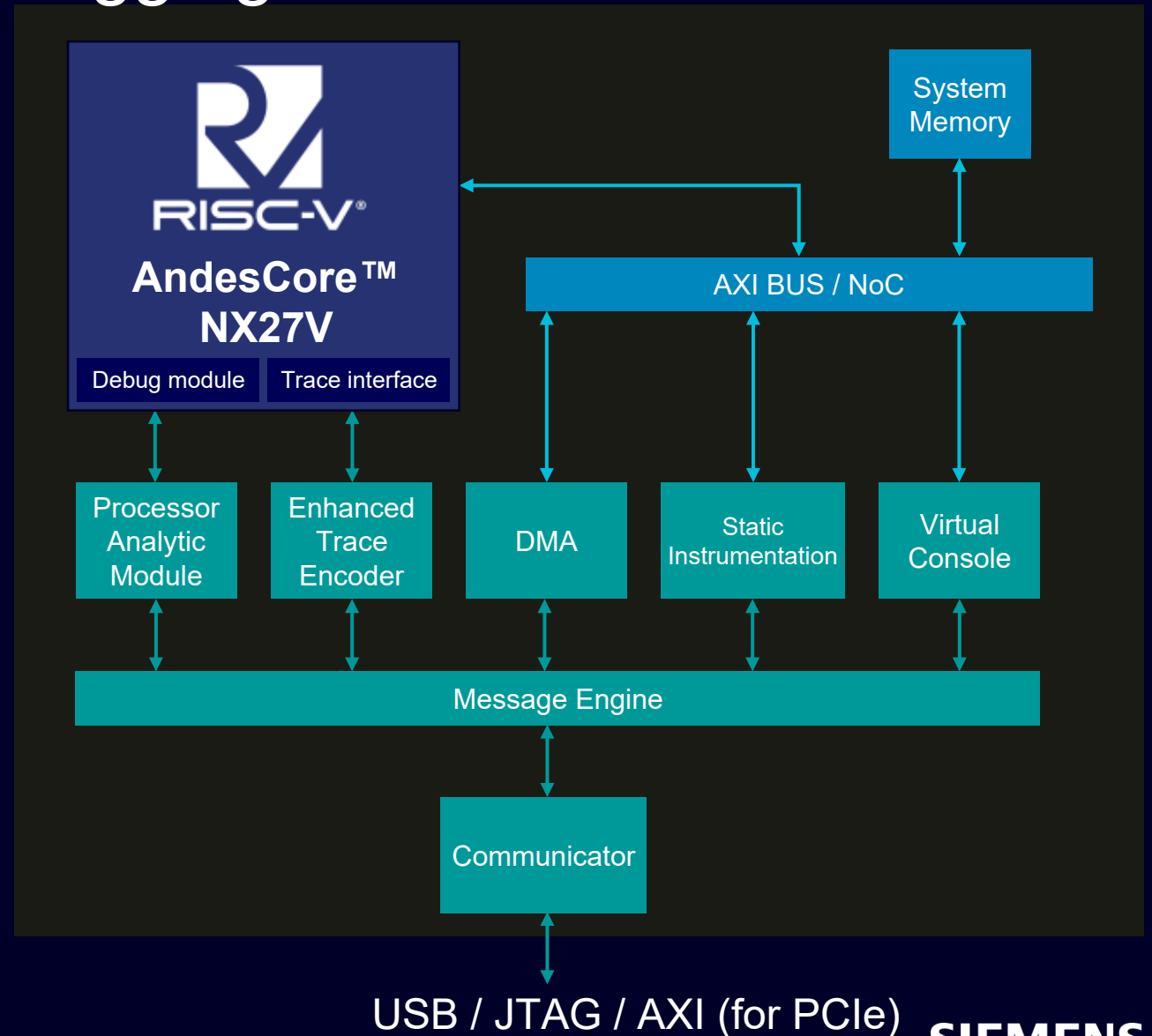
- DMA
  - Fast memory access
- Static Instrumentation
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- Virtual console
  - Replaces UART interfaces
- Messaging Engine
  - Scalable solution
- Communicators
  - Supports USB/JTAG/AXI (for PCIe)



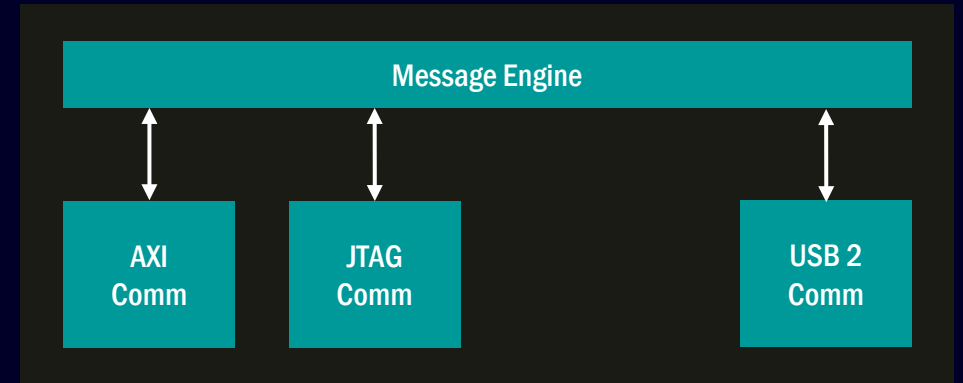
# Hardware IPs for Efficient Debugging

## Hardware IPs (Parametrized RTL)

- DMA
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  - Scalable solution
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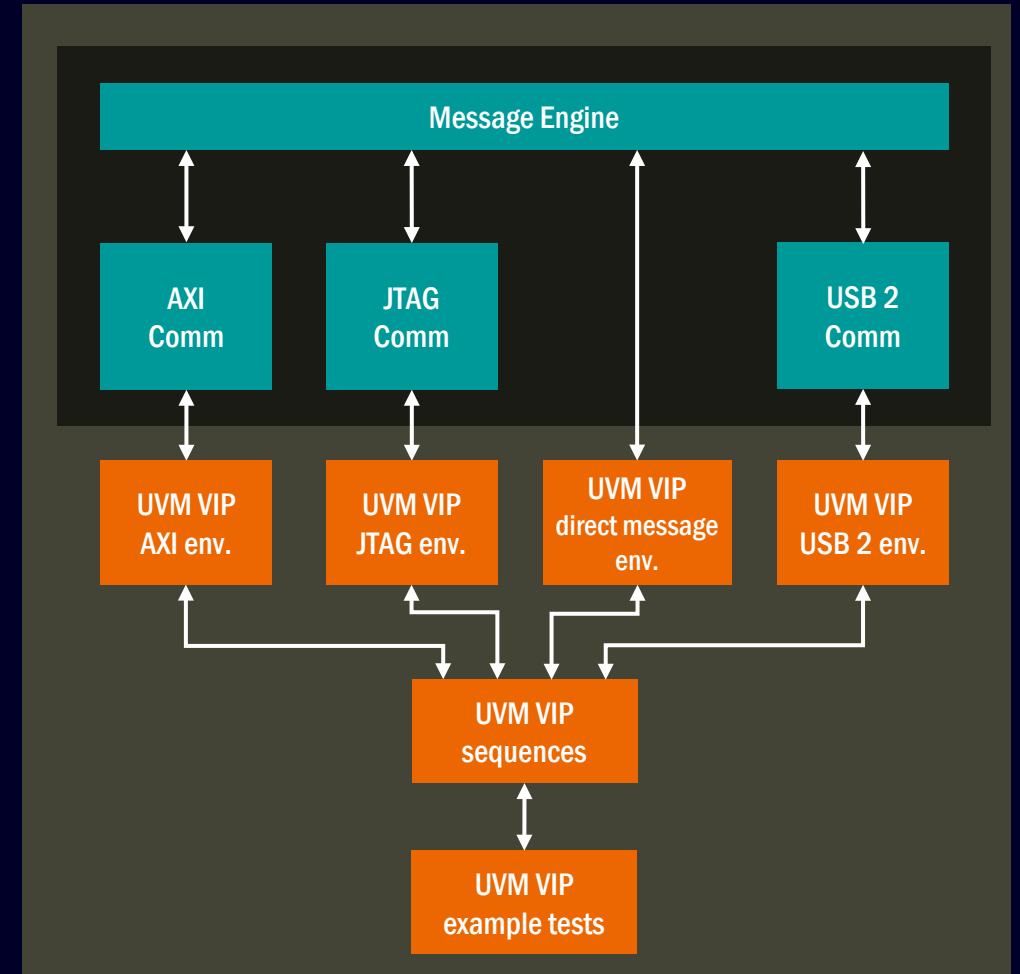


# UVM Verification IPs



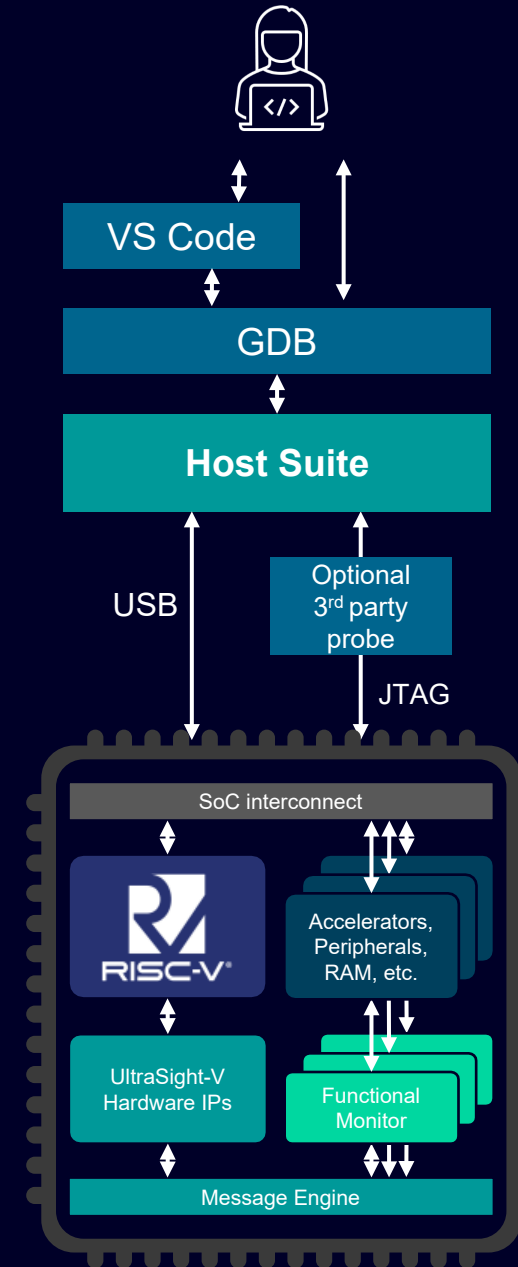
# UVM Verification IPs

- Verifies that UltraSight-V hardware IPs are correctly connected to each other and the SoC components
- UVM integration environment
- Virtual interfaces for each communicator IP
- Example test benches



# Software Environment

- Runtime control and trace using GDB and OpenOCD
- Integration with common IDEs (e.g. VS Code, Eclipse) or CLI
- Supports USB, JTAG, and AXI communication interface
- Supports RISC-V extensions and custom instructions



# Run Control and Trace

## IDE Support

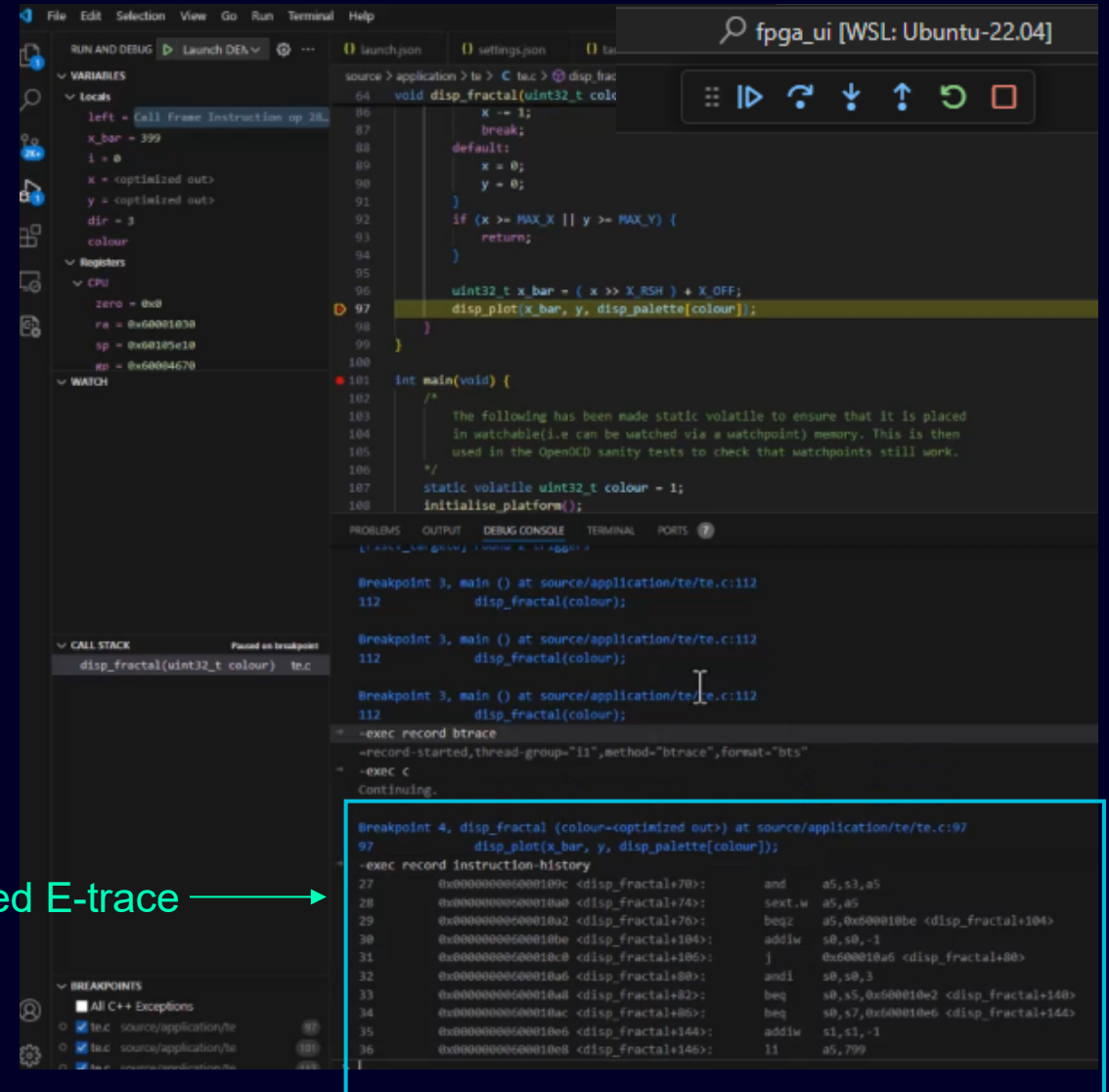
- Compatible with Visual Studio Code

## Run-control

- Comprehensive support of RISC-V is enabled through GDB and OpenOCD

## E-trace

- Instruction trace reconstruction to ASM and C via GDB
- Custom instructions support



# Efficient Debugging Features

## Fast code upload – “fast-load”

- Uses DMA
- Can be **up to 100x faster** than normal GDB load

## Minimal overhead logging

- printf style debugging with timestamps
- Can take as little as **a few instructions** (compared to printf at hundreds instructions)

## Virtual Console

- Interact with embedded software using UART-like capabilities (e.g. telnet)

The screenshot shows a debug console with the following output:

```
PROBLEMS 6 OUTPUT DEBUG CONSOLE TERMINAL PORTS 7 Filter (e.g. text)
+ -exec load
Loading section .init, size 0x290 lma 0x60000000
1018+download,{section=".init",section-size="656",total-size="1102771"}
1018+download,{section=".init",section-size="656",total-size="1102771"}
Loading section .t
1018+download,{sec
Loading section .r
1018+download,{sec
1018+download,{sec
Loading section .s
1018+download,{sec
Start address 0x0000000060000000, load size 12552
transfer rate: 7 KB/sec 3138 bytes/write.
+ -exec source /home/ /RISCV_NA_DEMO/hs_workspace/openocd/extensions/ea.py
+ -exec fastload
DMA opened successfully, mod_idx = 10, rpc_handle = 0
transfer rate: 483 KB/sec
> -|
```

A teal text box is overlaid on the screenshot with the text: "Fastload using the EA DMA is significantly quicker than gdb load".

## Instrument code with printf-style logging macros

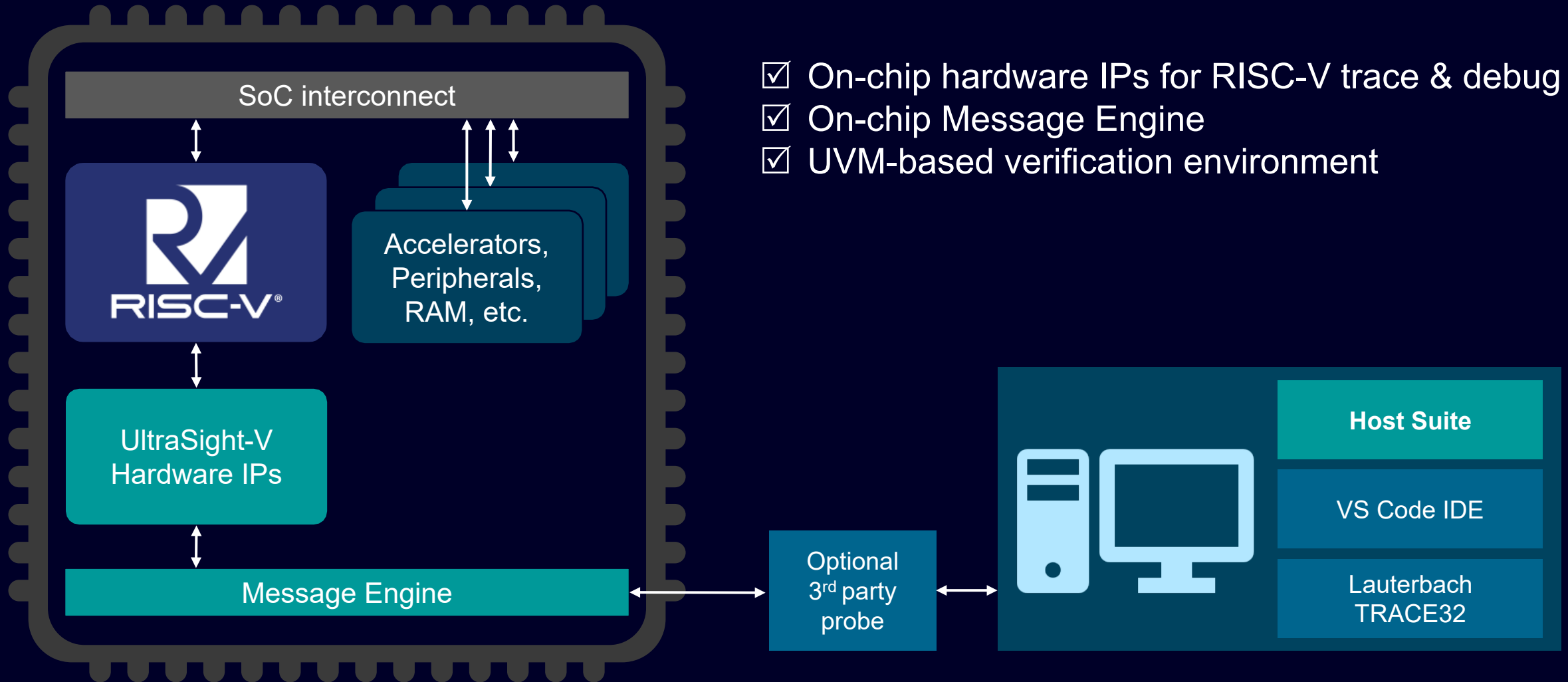
```
static void setup( void )
{
    USR_FUNCTION_ENTRY( setup );
    USR_LOGGING_INFO_STRING( "start me up" );

    smb_write_count_gap = 0;
    UST_LOGGING_DEBUG_PARAM3( "Pixel write y=%d, x=%d, colour=%u", y, x, colour );
}
```

**End-to-end RISC-V  
Debug and Trace  
Solution**

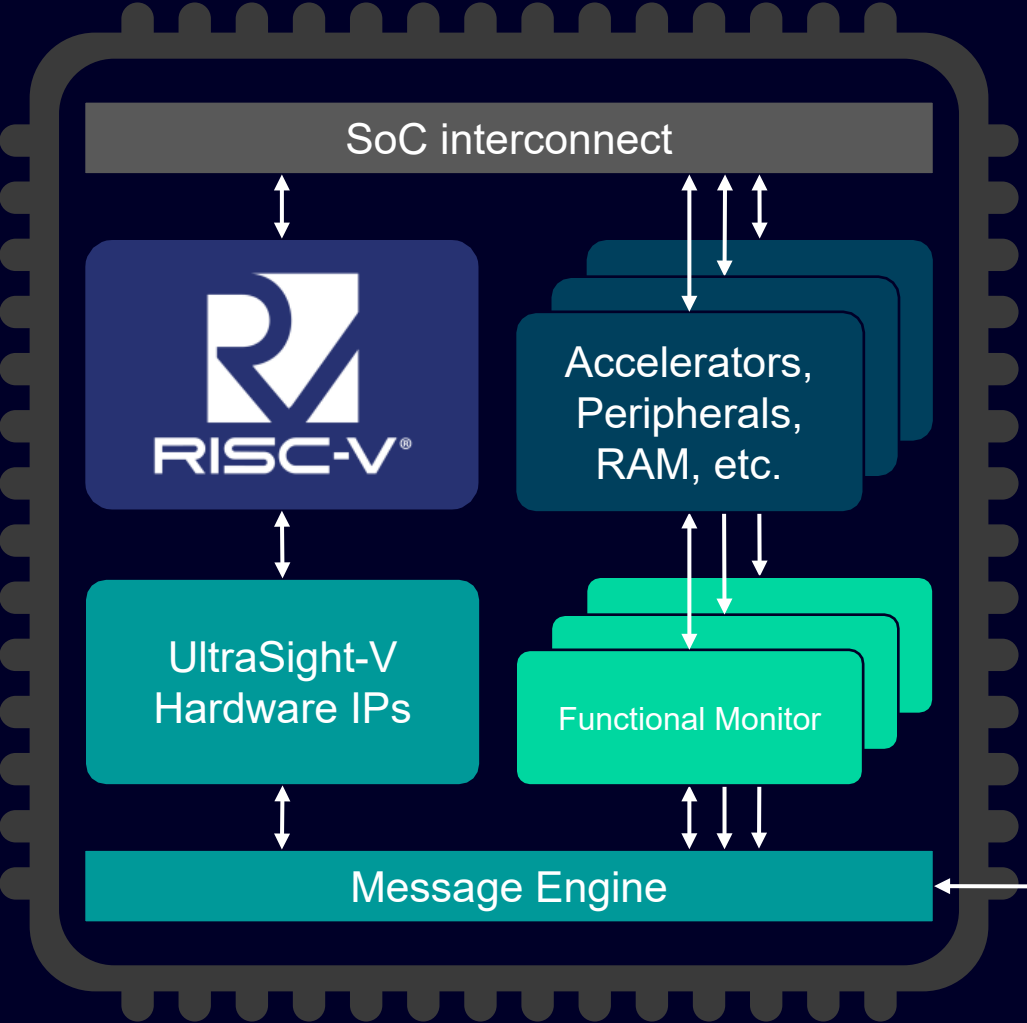
**Scalable to  
System-wide Debug**

# Scalable to full system debug



- ✓ On-chip hardware IPs for RISC-V trace & debug
- ✓ On-chip Message Engine
- ✓ UVM-based verification environment

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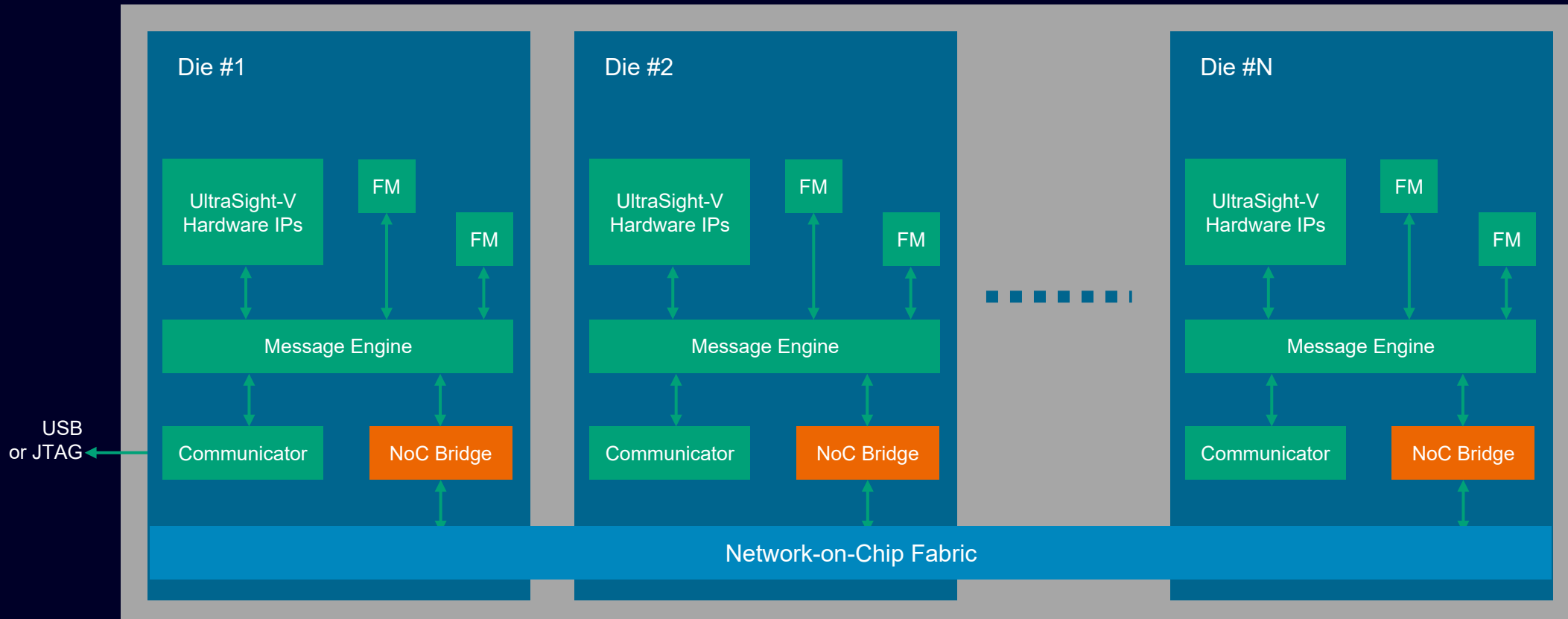


- ✓ On-chip hardware IPs for RISC-V trace & debug
- ✓ On-chip Message Engine
- ✓ UVM-based verification environment
- ✓ **Embedded Analytics Functional Monitors**



# An Example - Scale to Multi-Die Design

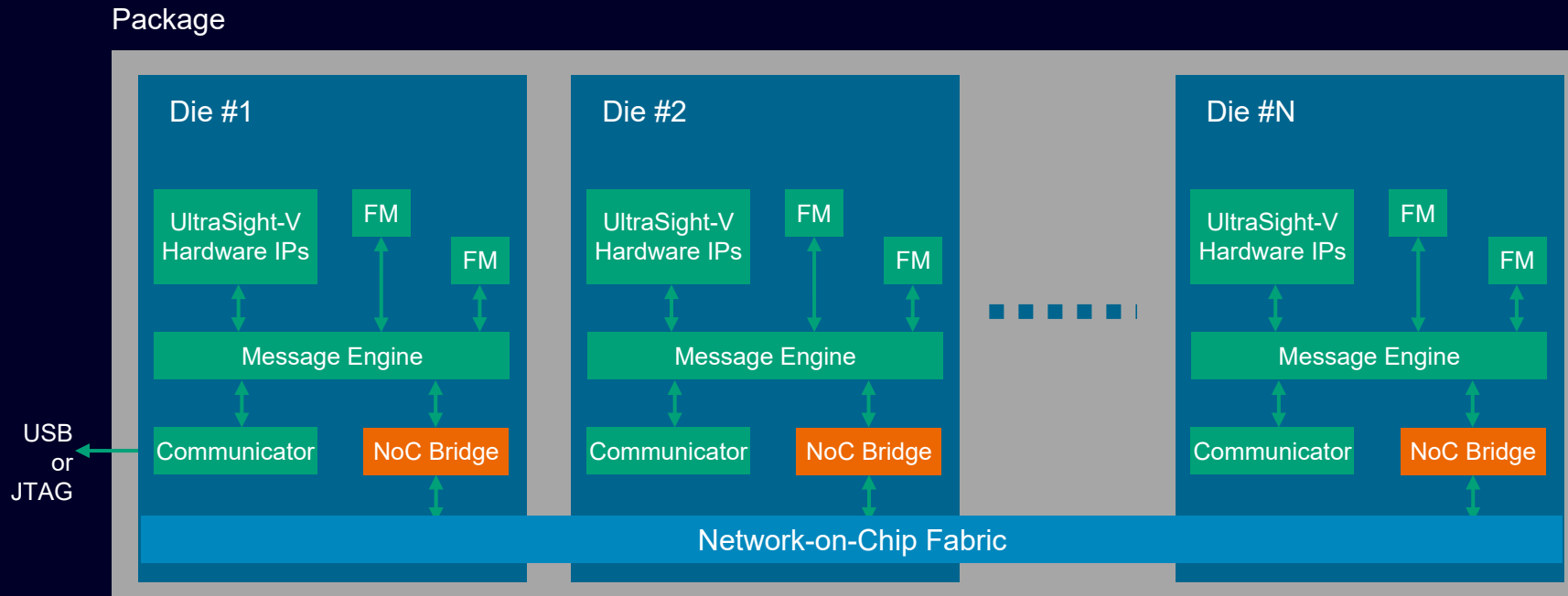
Package



FM Embedded Analytics Functional Monitor

# Scale to Multi-Die Design

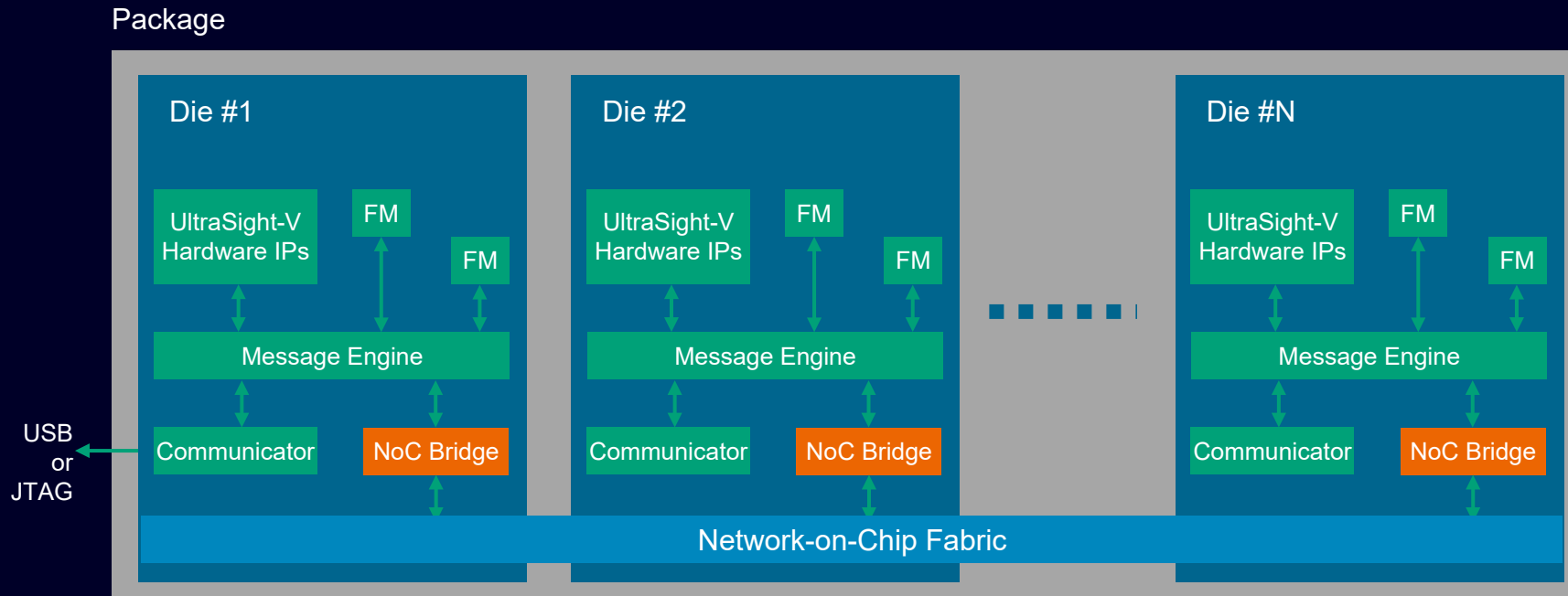
Extends visibility in multi-die systems



# Scale to Multi-Die Design

Extends visibility in multi-die systems

Any die can utilize Functional Monitors (FM)

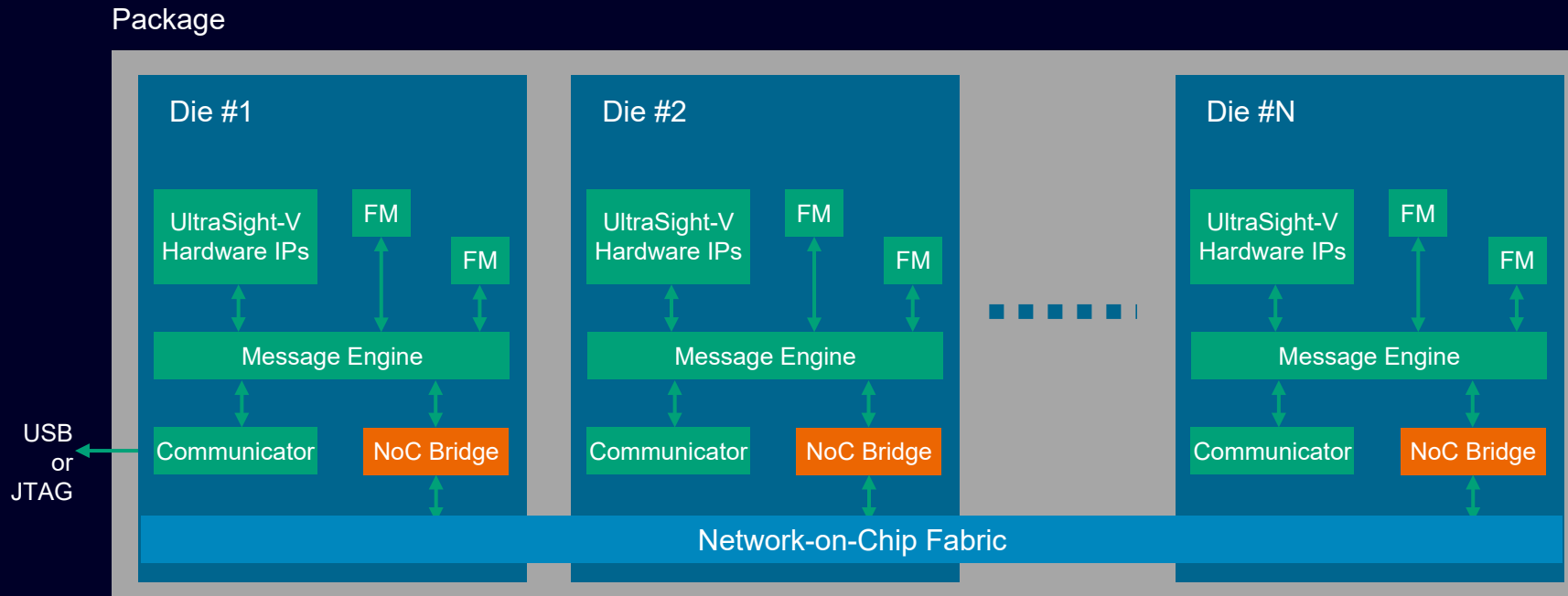


# Scale to Multi-Die Design

Extends visibility in multi-die systems

Any die can utilize Functional Monitors (FM)

Methodology proven for multi-die design



# Why Tessent UltraSight-V

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End-to-end RISC-V  
Debug & Trace Solution  
Reducing your time to market



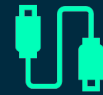
## Code Debug

- Run Control
- Fast memory access
- Instrumentation



## Efficient Trace

- Highly-compressed instruction trace (E-trace)



## Interface Options

- JTAG
- USB
- AXI (for PCIe access)



## Software Toolkit

- Supports VS Code IDE
- UVM Verification IP

# Why Tessent UltraSight-V

End-to-end RISC-V  
Debug & Trace Solution  
Reducing your time to market

Scalable to  
System-wide Debug  
Enabling you to future-proof your design



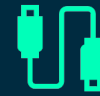
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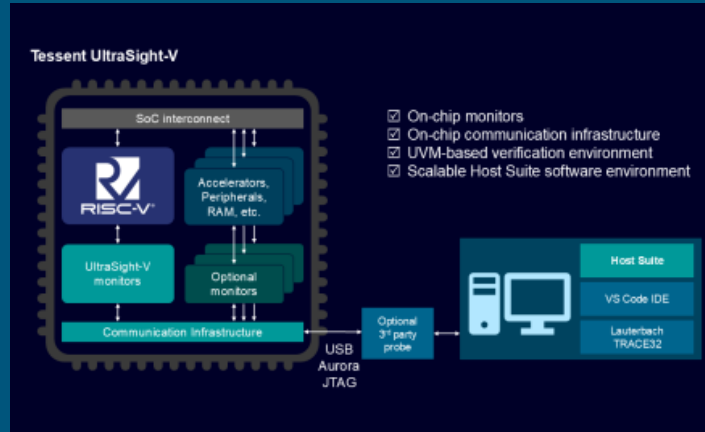
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# Learn more

[www.siemens.com/tessent/embedded-analytics/](http://www.siemens.com/tessent/embedded-analytics/)

## Tessent UltraSight-V

Learn more about the Tessent UltraSight-V solution, factsheet and video demo available



## Webinar RISC-V debug made easy

How Tessent UltraSight-V and Lauterbach TRACE32® work together to simplify RISC-V system debug

**SIEMENS LAUTERBACH DEVELOPMENT TOOLS**

RISC-V system debug and analysis made easy with **Lauterbach TRACE32** and **Tessent Embedded Analytics**

Tue, 8 Oct | LIVE Session 1 | 11am CEST  
Tue, 8 Oct | LIVE Session 2 | 9am PDT  
With **FREE REGISTRATION**

Lauterbach TRACE32

M. Sc. Michael Schleinhofer  
System Engineer,  
Lauterbach GmbH

Mike Sharp  
Product Engineer, Siemens  
Tessent Embedded Analytics

## Technical presentation RISC-V Trace

An overview of the Efficient Trace (E-Trace) standard and how processor trace is used to improve embedded software and applications.

**Leveraging the RISC-V Efficient Trace (E-Trace) standard**

Iain Robertson, Senior Engineering Director,  
Tessent Embedded Analytics

**RISC-V SUMMIT**

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## Case study Seagate

How Seagate Technology use Tessent Embedded Analytics products to improve debug and optimization challenges in their RISC-V SoCs.

Tessent Embedded Analytics IP provides visibility into the behavior of the whole SoC, not just the CPU, which is key in multi-CPU and heterogeneous processor systems

**Motion Control Use Case**

**The Problem**  
Hard drive capacity rapidly expanding  
At 50TB, track density will exceed 1 million tracks per inch (TPI) (2.4 nm positioning accuracy)

**The Required Innovation**  
Multi-stage actuators for coarse movement and fine positioning

**Real-Time Processing**  
• Disturbance detection algorithms  
• Adaptive control features  
• Feed-forward compensation  
• High sample-rate computation

**Constraints**  
• Power, space, and cost

**RISC-V-Enabled Solution**  
Functional Example: Disturbance detection filter (computational cycles)

Legacy Core  
Seagate RISC-V Core

Microarchitecture optimization, parallelism, and latency reduction

**SEAGATE RISC-V**

# Thank you

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